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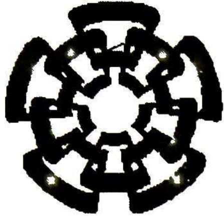

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Metodologías TCAD para diseñar diodos epitaxiales de recuperación rápida de silicio usando una estructura con contacto tipo mosaico P^+/N^+

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Metodologías TCAD para diseñar diodos epitaxiales de recuperación rápida de silicio usando una estructura con contacto tipo mosaico P^+/N^+

Tesis de Maestría en Ciencias
Ingeniería Eléctrica

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Resumen

La implementación de nuevas topologías de circuitos, así como el aumento en la frecuencia de conmutación han marcado la tendencia en el desarrollo de nuevos dispositivos semiconductores. Hoy en día, los rectificadores de potencia juegan un papel importante, tanto en las nuevas topologías como en aplicaciones de alta frecuencia. En particular, los rectificadores basados en estructuras P-i-N, requieren manejar densidades de corriente grandes (polarización directa), voltajes de ruptura elevados (polarización inversa), además de tener un tiempo de respuesta adecuado cuando se presenta una transición de polarización directa a polarización inversa (conmutación). No obstante, los diodos P-i-N convencionales de silicio tienen corrientes de recuperación inversa grandes y por consiguiente perdidas grandes durante la conmutación. Existiendo siempre un compromiso entre estas propiedades.

Teniendo en cuenta los requerimientos para el diseño de estructuras P-i-N, esta tesis investiga la posibilidad de usar un contacto tipo mosaico con regiones P^+ y N^+ para mejorar las características eléctricas de un Diodo Epitaxial de Recuperación Rápida (FRED, por sus siglas en inglés). Para ello, se propone una estructura P-i-N modificada con el contacto tipo mosaico situado en el ánodo (M-MCPD, por sus siglas en inglés). Esta estructura hace posible aumentar el voltaje de bloqueo sin sacrificar la caída de voltaje en directa. Entre las posibles aplicaciones para los M-MCPDs se encuentran: Diodos de giro libre, de sujeción, así como rectificadores en fuentes conmutadas.

El objetivo principal de los M-MCPDs es determinar la posibilidad de eliminar los procesos asociados con el control de tiempo de vida (contaminación con Platino) en diodos P-i-N actuales para mejorar su velocidad de respuesta. Con el fin de evaluar el desempeño del M-MCPD, se comparan los resultados obtenidos con un diodo P-i-N modificado (M-PiN) con un contacto convencional P^+.

Debido al enfoque del diseño asistido por computadora, el modelado de los FREDs se desarrolla usando el simulador de modelos numéricos ***ISE-TCAD** –Integrated Systems Engineering-Technology Computer Aided Design AG–*, el cual realiza la simulación tecnológica, eléctrica y en modo mezclado del dispositivo en 2-D. Los modelos basado en la física del semiconductor emplean procesos de manufactura estándar y datos de la geometría estructural de un dispositivo comercial.

Los resultados de la simulación demuestran que, las características dinámicas en los M-MCPD se pueden controlar cambiando la razón de área P^+/N^+ en al mosaico, como lo hace la variación del tiempo de vida de los portadores minoritarios en los rectificadores P-i-N convencionales a través de la difusión de Platino. Como las diferentes razones de área del mosaico no afectan considerablemente las características en directa del M-MCPD, comparado con el rectificador M-PiN, el M-MCPD presenta un mejor compromiso entre la caída de voltaje en directa y el tiempo de recuperación en inversa.

Finalmente, con el fin de validar el modelo físico del rectificador de potencia, se utilizaron resultados experimentales de un diodo "ultrafast" convencional disponible comercialmente. Los resultados obtenidos en las simulaciones mostraron ser congruentes con los datos medidos del diodo "ultrafast" convencional.

Abstract

New circuit topologies and a tremendous increase in switching frequencies, have been the driving factors of the development of improved semiconductor devices. Power rectifiers are today playing a key role in this new topologies and in high-frequency applications. In particular, for P-i-N-based rectifier structures, it is required to conduct large current densities (forward-biased) and high breakdown voltages (reverse-biased), as well as having an appropriate transient response. However, conventional silicon P-i-N diodes have large reverse recovery currents and hence, large switching losses. There is always a trade-off between these properties.

This thesis investigates, taking into account the design requirements for P-i-N diode structures, the possibility of using a P^+/N^+ type-mosaic contact to improve the electrical characteristics of **F**ast **R**ecovery **E**pitaxial **D**iodes (FREDs). For this, a Modified Mosaic Contact P-i-N Diode (M-MCPD) structure was proposed. The mosaic contact is placed on the anode side. This structure makes possible to increase the blocking voltage without sacrificing the forward voltage drop. M-MCPDs are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications.

M-MCPDs are aimed of determining the possibility of eliminating processing associated with lifetime control (Platinum-doped) used to improve the switching speed in current P-i-N diodes. To evaluate the device performance, the results are compared to a modified P-i-N rectifier (M-PiN) using a conventional P^+ contact.

Because of the aimed Computer-Aided Design approach, FREDs models are developed in the ***ISE-TCAD –Integrated Systems Engineering-Technology Computer Aided Design** AG–* device simulator that employs 2-D technological, electrical and mixed-mode simulators that use numerical modeling approach. The physical-based power rectifier model is based on standard manufacturing processes and device structural geometry information from a commercially available rectifier.

Numerical simulation results demonstrate that changes in the P^+/N^+ mosaic ratio in the M-MCPD rectifier can be used to control its switching characteristics in a similar manner to variations of the minority carrier lifetime by Platinum doping used in conventional P-i-N rectifiers. Since the forward voltage drop of the M-MCPD is not quite affected by different mosaic area ratios the M-MCPD rectifier exhibits a better trade-off between forward drop and switching characteristic compared to the M-PiN rectifier.

Finally, experimental results were used to validate the physical-based power rectifier model. The results obtained from the simulations were shown to be in close agreement with the measured data of the conventional ultrafast rectifier.

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heav

Preface

Motivation

THE development of power electronics systems based on semiconductor devices can be traced back to the early 1950's. At that time, the first rectifiers capable of operating at high current and voltage levels were introduced into the marketplace. During the following 30 years, the technology for these bipolar devices reached a high degree of maturity. However, today's power semiconductor industry requires highly efficient rectifiers for a wide range of applications.

Circuit designers need low-loss power rectifiers for both conduction mode and dynamic mode operations, especially in high-frequency applications (>100Khz). The reason for this is that power rectifiers must process power with a minimum power loss in operating conditions that often cover a wide range of blocking voltages, current densities, and frequencies.

While the Schottky diode is an ideal low voltage fast switching device, it cannot sustain high blocking voltages. Higher reverse voltage and forward current density operation requires a P-N structure. Bipolar junction rectifiers can block voltages up to 1500V and have current capability up to 100A. One of the main problems here is that for switching applications, a bipolar junction rectifier is much slower than a Schottky due to the need to remove the stored charge from the base during turn-off.

The switching process can be accelerated by reducing the minority carrier lifetime using different techniques such as Gold doping, Platinum doping or electron irradiation. Nevertheless, these approaches have the adverse effect of reducing conductivity modulation in forward-bias and hence increasing the forward voltage drop. This can lead to a dramatic increase in forward conduction losses. Consequently, there is a compromise between switching speed and forward voltage drop which has been the main topic of many investigations. High leakage effects that generate a significant proportion of devices fail to pass blocking voltage specification could also appear.

It is of great interest to find a solution to guarantee a fast transient response of power rectifiers without using lifetime killing approaches.

One such study that shows techniques to minimize the secondary effects was carried out by Amemiya *et al.* [1], which used a P^+/N^+ "ideal" ohmic contact or mosaic contact to increase the switching speed of an epitaxial diode consisting of a lightly doped P-type epi layer on N^+ substrate. Instead of using a standard P^+ contact to the epi layer, a mosaic with P^+/N^+ regions was used, which facilitated the removal of the minority carriers, electrons in this case, from the epi. The authors reported a factor of ten improvement in switching speed for non-inductive test circuit. A considerable improvement in the forward voltage drop and in the leakage current was also observed. No lifetime control was used.

The motivation for developing this thesis is to investigate the possibility of using a similar P^+/N^+ mosaic to improve the electrical characteristics for high speed power rectifiers. In this work, a modified Mosaic Contact P-i-N Diode (M-MCPD) suitable for monolithic combination with a transistor is studied. The generation of an M-MCPD with a conventional epitaxial process (with an N-type epitaxial layer grown on an N^+ substrate) consists of a lightly doped N-type epitaxial layer between the N^+ substrate and a diffused P-region where the anode mosaic contact is placed.

Since at the present time semiconductor devices cannot be manufactured without having been simulated to predict the possible behavior that they will have in real life, the simulation has become a standard tool in electronics, moreover it allows a qualitative and quantitative analysis of the device. Therefore by using such tools, the designer can get a considerable saving in time, as well as in cost, compared with the use of a conventional experimental runs to carry out tests and evaluations. The simulation is more effective and faster. This tendency eliminates many trails prior to fabricate prototypes until the specifications are fulfilled, providing the reliability of the design for its production. In order to carry out a detailed numerical analysis of the devices under study, without need to manufacture it, technological process simulation was used, as well as the device simulation, including electrical and mixed-mode (circuit/device) techniques.

The simulation software of 2-D technological semiconductor process and electrical characteristics behavior available at **CINVESTAV-IPN** Guadalajara Unit belongs to ***ISE-TCAD*** *–Integrated **S**ystems **E**ngineering-**T**echnology **C**omputer **A**ided **D**esign AG–* programs.

Objective

The main objective of this thesis is to evaluate the possibility of matching, or even improving, the steady-state and dynamic specifications of actual Platinum-doped high-speed power rectifiers with a proposed Mosaic Contact P-i-N Diode structure without using lifetime killing, employing a technology computer aided design approach.

In order to accomplish the main objective of this research is necessary to develop the following activities:

- To develop a systematic design methodology that relies on device and circuit simulator programs to design and optimize silicon-based semiconductor devices.
- To depict the P-i-N diode behavior, including the physical models of recombination mechanisms and its transport models (e.g., drift-diffusion model).
- To design, simulate and analyze a power rectifier diode (P-i-N-based structure) with an "ideal" ohmic contact, which has a P^+/N^+ regions mosaic layer, to control the base region stored charge.

Methodology

To carry out the suggested activities, the procedure was as follows:

a) Bibliographic review. A summary of the existent information regarding the topic of investigation was considered in order to determine the feasibility of the proposal.

b) Study of operation and fundamental parameters of P-i-N diode structures. Through this study, it could be known which parameters to fulfill the design specifications should be optimized; e.g., forward voltage V_F, breakdown voltage V_{Br} or reverse recovery time t_{rr}.

c) Study of ISE-TCAD's simulation programs to determine their facilities and advantages. Through this study, general aspects of simulation and device semiconductor modeling were analyzed. This part focuses on power semiconductor devices for both their technological manufacturing process (starting substrate, epitaxial growth, diffusion, deposition, etc.) and their electrical characteristics (I-V curves, switching speed, etc.)

d) Development of a systematic **TCAD** design methodology applied to a case-of-study regarding power semiconductor rectifier structures.

e) Design and simulation of Fast Recovery Epitaxial Diodes (FREDs) with a conventional P^+ contact and a P^+/N^+ mosaic contact, with the aim of verifying the benefits and limitations that a mosaic-type contact provides compared to a conventional one.

f) Validation of simulation results. Here, the results from the electrical a mixed-mode simulations are compared to experimental results from a commercially available power rectifier. Hence evaluate the numerical modeling and justify their industrial level production.

Thesis Organization

This dissertation is organized as follows:

In the ***Introduction***, a general overview of the applications for power semiconductor devices is presented, as well as a review of resent trends in low- and high-voltage power rectifiers. Following this, mosaic-type ohmic contact structures are introduced. ***Chapter 1*** deals with fundamental considerations such as lifetime, emphasis is placed on recombination processes. Power P-i-N diode at different injection levels for the on-state condition is treated. The reverse-bias operation characteristics, including a design criteria for breakdown voltage will be discussed, as well as the basic mechanisms for current flow under reverse blocking conditions. ***Chapter 2*** is a review of power rectifier reverse transient physics, including both step and ramp reverse recovery process. In ***Chapter 3***, a TCAD design methodology that supports physical modeling for semiconductor devices is presented. A detailed description of programs, and main physical models implemented in the numerical simulator are provided. ***Chapter 4*** discusses simulation results of forward voltage drop, breakdown voltage, reverse leakage current and reverse recovery of the power rectifier diode structures under study. These results are analyzed and compared to experimental results. ***Chapter 5*** contains a summary of key results, and recommendations for future developments in order to optimize P-i-N-based rectifier structures presented in this work. ***Appendix A*** provides a review of the conventional diffusion models, as well as the growth of monocrystalline silicon layers (epitaxy) used in technological simulations. ***Appendix B*** includes the simulation input command files used to generate the ISE-TCAD simulations. ***Appendix C*** presents the list of publications as a result of this work.

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Chapter 0

Introduction

A general overview of the applications for power semiconductor devices for both, power ratings as a function of system operating frequency and power handling capability, as well as in relation of their voltage and current ratings is presented. Trends and the state-of-the-art focused on power rectifiers will be pointed out. Finally, the mosaic contact P-i-N diode structures are introduced.

0.1. Introduction

POWER semiconductor devices (PSDs) play a crucial role in the regulation and distribution of power and energy in the world. Consequently, the performance of power discrete devices used in systems has a significant impact on the efficient use of electricity. In the power electronics community, it is well recognized that the improvements in system performance in terms of efficiency, size, and weight are driven by enhancements made in semiconductor device characteristics. With the support of the world-wide power semiconductor industry, major advances in silicon technology have been obtained to create improved power rectifiers and switches for the near term [2].

The roots of power semiconductor device technology extend before those for integrated circuits (ICs). Since the invention of the bipolar transistor and the thyristor, there has been a strong motivation to increase the power handling capability of power discrete devices in order to extend their applications.

Applications that have provided a technology pull for power discretes are in computers, telecommunications, an automotive industries for devices operating at below 200 volts; and motor control, robotics, an power distribution for devices operating at above 200 volts.

0.2. Power Semiconductor Device Applications

The applications for power devices extend over a very large range of power levels and frequency. Some of these applications are shown in the power frequency spectrum illustrated in *figure* 0.1. From this figure, it can be seen that the power levels demanded by the system are generally higher at lower frequencies. Some examples of areas in which the new device technology is expected to play an important role are automotive electronics, switching power supplies, factory automation, new higher-efficiency lighting systems, and appliance control for the electronic home of the future.

Some of the prominent applications for PSDs are shown in *figure* 0.2, where boxes indicate the device voltages and current ratings required to meet the system needs. It is obvious that the device ratings span a very broad range of voltages and currents. At relative low voltages (<100V), two important applications are in power supplies for computers, telecommunications or office equipment, for automotive electronics.

As indicated in *figure* 0.2, there are applications, such as displays and telecommunications circuits, for power devices operating at relatively low currents (<1A). Turning to the high power end of the applications spectrum (>100V), devices are needed for traction (electric street-cars and locomotives), and for power distribution networks.

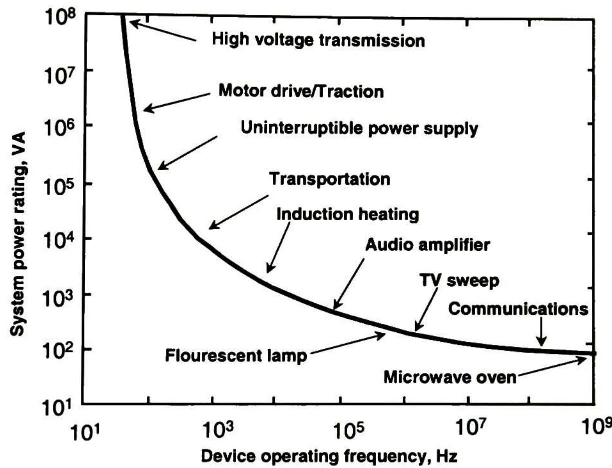


Figure 0.1: *Applications of power semiconductor devices. Power-frequency spectrum [3].*

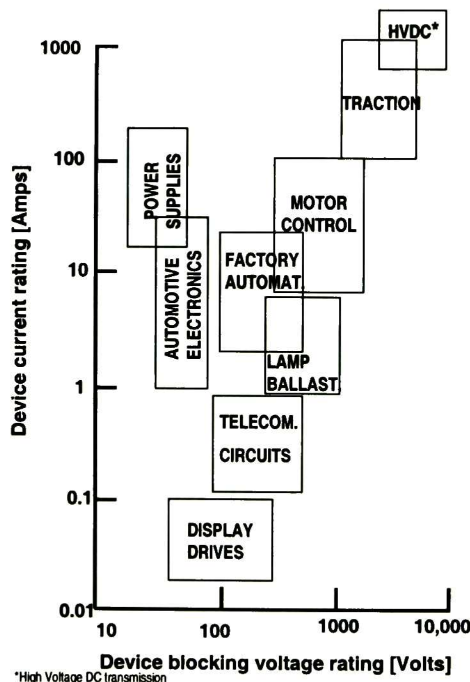


Figure 0.2: *Application for power semiconductor devices. Device voltage and current ratings [4].*

Power electronic circuits are involving toward higher operating frequencies to improve their compactness -reduction in the size of the passive components- and efficiency. This is mainly due to the introduction and improvement of new devices with low-on-state voltage drop and high-switching speed such as the power MOSFET [5], the insulated gate bipolar transistor (IGBT) [6], the family of MOS-gated thyristors and power field-controlled diodes (FCD) [7], For instance, today's IGBTs are robust, with always low on-state voltage drop. In low-power range, fast three terminal devices with switching frequency grater than 100kHz are currently available.

As a consequence, other devices, such as the P-i-N rectifier, became the weakest part of power circuits, and very often power circuits performance is limited by the power rectifier. This circuits need faster rectifiers able to work in a hard-switching topology with low static and dynamic losses.

0.3. Power Rectifier Diodes

Power rectifiers are needed for all the applications shown in *figure* 0.1 and *figure* 0.2. During the 1950´s, the P-i-N rectifier (usually called First Recovery Diode, FRD) was commercially introduced for power electronics applications. Since then, there have been continuous improvement in the rating of these devices based upon the demand for them in power applications. In addition, new device structures have been introduced in order to improve their switching performance [8-12]. The silicon device structure that has been found to be the most suitable for each application depends upon the voltage rating of the rectifier.

Almost all of the power semiconductor diodes manufactured today are made up around the same type of P-i-N structure. This basic structure allows semiconductor manufacturers to offer the widest range of performance and characteristics, such as blocking voltage capability, forward voltage drop and switching speed, by means of the control of the following key elements:

- Die size.
- Die thickness.
- Field termination structure.
- Base width.
- Doping level.
- Recombination lifetime control.

While the first two elements have a clear and direct effect on diode performance, the latter have influence over the characteristic of the diode's region (base) that separates the highly doped P and N regions, and that controls the dynamic (switching) and static (on-state) performances of the device.

The ideal fast power diodes must be able to support a low forward voltage drop , high breakdown voltage and low leakage current, short reverse recovery time, low reverse recovery charge, a suitable shape of reverse recovery current (soft recovery), and a low forward recovery voltage. Although much progress has been made in striving towards these goals, the ideal rectifier continues to elude the power semiconductor designer. Providing strong motivation for further research and development in this area.

0.3.1. Low Voltage Power Rectifiers

Power rectifiers with reverse blocking capabilities of less than 100V are required for application such as a switch mode power supplies and automotive electronics; see *figure* 0.2. The first devices available for these applications were germanium rectifiers. However, the high leakage currents in germanium devices associated with its small energy bandgap (0.66eV) lead to its replacement by silicon P-i-N rectifiers (1.12eV) [13].

The basic P-i-N rectifier structure is shown in *figure* 0.3. The doping concentration and thickness of the drift-region is designed to support the required reverse blocking voltage. During on-state current flow, the P^+ and N^+ regions inject a high concentration of holes and electrons into the drift-region, when the applied bias exceeds the junction built-in potential, leading to an increase in its conductivity. This is responsible for the on-state voltage drop of the P-i-N rectifier being close to 1V for these low breakdown voltage structures. When the voltage across the device reverses polarity, the injected electron-hole population (called stored charge) must be removed before the formation of a depletion region can occur to support the reverse blocking voltage. This leads to a reverse recovery current that is typically equal in magnitude to the on-state current. The presence of a reverse recovery transient leads to power dissipation that limits the maximum switching frequency for P-i-N rectifiers.

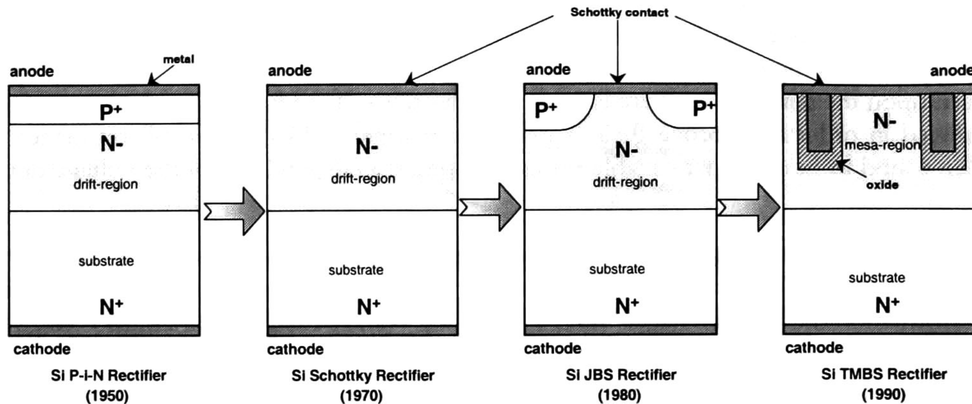


Figure 0.3: *Evolution of low voltage (<100V) power rectifiers.*

In order to eliminate the reverse recovery problems associated with P-i-N rectifiers, the Schottky barrier diode (SBD) was developed in the 1970's [7]. As shown in *figure* 0.3, its structure consists of a metal-semiconductor rectifying contact with a N^- drift-region which is designed to support the required reverse blocking voltage. Forward conduction in the SBD occurs by the transport of electrons across the metal-semiconductor barrier. The on-state voltage drop of the SBD consists of the sum of the voltage drop across this barrier and the ohmic voltage drop across the N^- drift-region.

By replacing the P-i-N rectifier with the SBD, it is possible to obtain a reduction in on-state power loss by a factor of two. In addition, a significant advantage of SBDs is their faster switching speed because of the absence of the reverse recovery current transient observed in P-i-N rectifiers, thus, allowing the operation of switch mode power supplies at higher frequencies.

The efficiency of switch mode power supplies has been found to be strongly dependent upon the voltage drop across the output rectifiers in relation to the output voltage. A 10 percent loss in efficiency occurs in the case of a 5V power supply with a conventional SBD having an on-state voltage drop of 0.55V, e.g., doping concentration of the N^- drift-region between 5×10^{15} and 1×10^{16} cm^{-3} with a thickness less than 10μm for state-of-the-art device [4]. It is therefore imperative that rectifiers be developed with lower on-state voltage drop.

One of these approaches is the junction barrier controlled Schottky (JBS) rectifier shown in *figure* 0.3. This structure consists of a SBD with a junction grid integrated under the metal-semiconductor contact. The junction grid serves to prevent Schottky barrier lowering, a phenomenon that produces poor reverse blocking characteristics with high leakage currents. JBS rectifiers have been fabricated with on-state voltage drops of 0.35V by using VLSI technology, [8, 10]. Further reduction in on-state voltage drop was not possible due to the area taken up by the junction regions.

An even superior low voltage power rectifier was conceived and experimentally demonstrated recently based upon incorporation of a trench MOS structure below the metal-semiconductor contact [11]. The cross-section of the TMBS rectifier is shown in *figure* 0.3. The charge coupling between the donors in the mesa region and the metal on the trench sidewalls produces a redistribution of the electric field under the metal-semiconductor contact. The TMBS structure offers benefits for improving the efficiency of power supplies with output voltages ranging from 5V down to 1.6V.

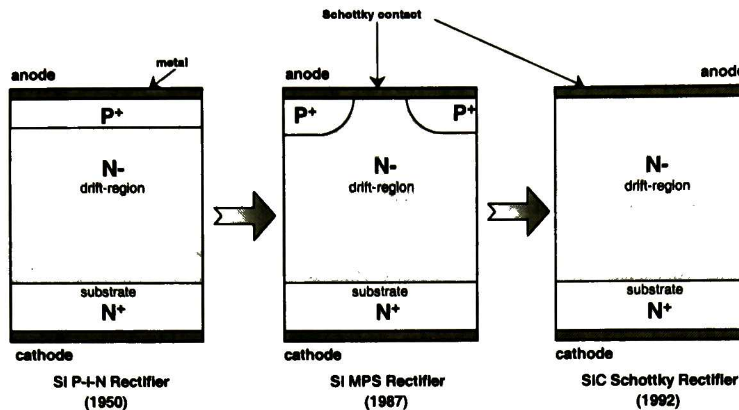


Figure 0.4: *Evolution of high voltage (>300V) power rectifiers.*

0.3.2. High Voltage Power Rectifiers

High voltage power rectifiers are needed for many applications such as motor control. Most commercial systems utilize the P-i-N rectifier structure shown in *figure* 0.4 which is essentially identical to the low voltage P-i-N rectifier shown in *figure* 0.3 with a wider drift-region to increase its reverse blocking capability. These devices are available with blocking voltages in excess of 5000V. Their primary drawback has been the large reverse recovery current flow during switching from the on-state to the reverse blocking state due to the large amount of stored charge in the drift-region. Many methods of lifetime control have been developed to reduce the lifetime in the drift-region to decrease the turn-off time but they all lead to an increase in the on-state voltage drop [14]. It is therefore customary to perform a compromise between on-state and turn-off losses when designing these devices.

Four major design techniques brought about this improvement [15-18]:

a) Deep Diffusion Control (Gold or Platinum doping).
b) Electron Irradiation.
c) Emitter Efficiency Control.
d) Axial Lifetime Killing Control.

Of course, any manufacturing process for ultrafast diodes has advantages as well as disadvantages. For example, diodes using Gold doping to control minority carrier lifetime, represent an excellent compromise between forward voltage, low peak reverse recovery currents with soft recovery. These diodes are characterized by a soft recovery behavior from -40°C to +150°C, showing even at very high rate of change $-di_F/dt$ (>800A/µs) no tendency to "snap-off" The higher leakage current of the Gold doped diode is, in comparison to the Platinum doped or irradiated diode, the only disadvantage. However in most applications, the power loss caused by the leakage current is small in comparison to forward current and reverse recovery losses.

A superior trade-off curve can be obtained by using the merged P-i-N/Schottky (MPS) rectifier structure shown in *figure* 0.4. Although the MPS structure appears to be similar to the JBS structure shown in *figure* 0.3, its physics of operation is different because of injection of minority carriers from the junction, a phenomenon that is absent for the JBS device. In the JBS rectifier, the on-state voltage drop is less than 0.5V making the junction potential insufficient for the injection of carriers. In the MPS rectifier, the on-state voltage drop is about 1V leading to the injection of minority carriers into the drift-region. This injection leads to a reduction in the resistance of the drift-region below the Schottky

contact allowing a large proportion of the on-state current to flow thorough the metal-semiconductor contact in the MPS rectifier. It has been shown that the MPS rectifier behaves like the SBD at on-state voltage drops of less than about 0.6V [9]. However, unlike the SBD whose on-state current becomes limited by the large series resistance of the drift-region, the on-state voltage drop of the MPS rectifier remains low due to the injection of carriers from the P-N junction at voltages above 0.7V.

Due to the process compatibility of the MPS rectifier with the P-i-N rectifier, it is anticipated that the MPS rectifiers will become widely available for commercial applications. It has been found by two-dimensional numerical simulations that the carrier distribution profile in the MPS rectifier results in a lower stored charge by a factor of upon eight times when compared with the P-i-N rectifier [9]. This produces a greatly reduced (4X smaller) reverse recovery current. However, these devices cannot be considered as ideal for power switching because they still exhibit a large leakage current, and a substantial reverse recovery transients. A much superior power rectifier can be created by using the metal-semiconductor rectifying contact if the resistance of the drift-region can be reduced, while preserving the high blocking voltage capability. An approach for achieving this was first proposed in 1982 by replacing silicon with a wide bandgap semiconductor [4]. Based upon this fundamental analysis, power devices based upon silicon technology are rapidly approaching their theoretical limits of performance. Consequently, it would be necessary to develop devices from other materials (gallium arsenide, silicon carbide, or semiconducting diamond) in the future in order to reduce power losses in high-frequency systems and to achieve high efficiencies.

For example, an even greater reduction in the resistance of the drift-region can be projected for silicon carbide; see *figure* 0.4. These devices have excellent switching behavior as expected with an on-state voltage drop of only 1 volt; thus, verifying the theoretical predictions. Although the cost of silicon carbide wafers is too high and the size of the wafers too small for commercial production of power SBDs. It is anticipated that all the silicon P-i-N rectifiers will be replaced by silicon carbide SBDs in the twenty-first century [19].

0.4. Mosaic-Type Contact

As mentioned above, there is a trade-off between switching speed and forward voltage drop which has been the subject of many investigations. One such study by Amemiya *et al.* [1] shows techniques to minimize the undesirable effect of reducing conductivity modulation in forward direction and hence increasing the forward voltage drop caused by the minority carrier lifetime control. As it can be seen from the evolution of power rectifiers, in the past, the contact to the drift-region of the N^+-P^- rectifier has been made by using a high concentration P^+ layer; see *figure* 5(a). The P^--P^+ interface produces an "ohmic" contact for majority carriers. The P^--P^+ contact creates an electric field due to the concentration gradient given by [7]

$$E = \frac{kT}{q}\frac{1}{N_A}\frac{dN_A}{dx} \tag{0.1}$$

where E is the electric field, k the Boltzmann's constant, and N_A the acceptor concentration. The presence of the electric field partially reflects any minority carrier (electrons in this case) that approach the interface [20] as illustrated in the band diagram shown in *figure* 5(a). In power rectifiers, the reflection of minority carriers can be detrimental to the achievement of fast turn-off because minority carriers become trapped in the drift-region and increase the stored charge.

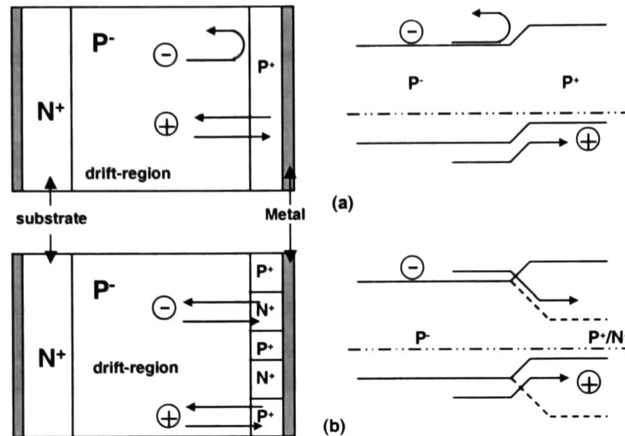


Figure 0.5: ***Structures and band diagrams: (a)Conventional P^--P^+ contact and (b)'Ideal' ohmic contact with mosaic P^+/N^+ regions. (After Amemiya et al.).***

To obtain an "ideal" ohmic contact, or "universal contact" (UC), that can simultaneously allow the transport of holes and electrons across its interface, a contact consisting of a mosaic of P^+ and N^+ regions has been proposed [1]. The improved structure consists of a P-type epitaxial layer on an N^+ substrate using an UC to terminate the lightly doped drift-region as shown in *figure* 0.5(b). In this contact, the N^+ regions provide an ohmic path for electrons while the P^+ regions provide the conventional ohmic path for holes.

The UC formed with the mosaic of the P^+ and N^+ regions and its composite band diagram are shown in *figure* 0.5(b). The authors reported a factor of ten improvement in switching speed for non-inductive test circuit. A considerable improvement in forward voltage drop and in leakage current was also observed. No lifetime control was used.

This work investigates the possibility of using a similar P^+/N^+ mosaic to improve the switching characteristics and so control the stored charge, employing the state-of-the-art epitaxy construction, in Fast Recovery Epitaxial Diodes (FREDs). FREDs are ideally suitable for high voltage and high frequency applications. The aim is to determine the possibility of eliminating the Platinum doping used to decrease the minority carrier lifetime to increase the switching speed in conventional structures.

In FREDs, the N-layer that supports the reverse voltage, should be made as thin as possible to minimize the forward voltage drop as well as the stored charge in the P-N junction. To obtain a wafer thickness that allows a good mechanical handling of the wafers, the epitaxial technology is the most favorable choice. This technology makes use of a relatively thick N^+ doped wafer substrate for mechanical strength, on which a thin, monocrystal N-layer (the so-called epitaxial layer), is grown. The epitaxial layer thickness and resistivity are adjusted according to the desired blocking voltage capability.

In this thesis, a modified Mosaic Contact P-i-N Diode (here called M-MCPD) structure is studied. It makes possible to increase the blocking voltage without sacrificing the forward voltage drop. The M-MCPD consist of a lightly doped N-type epitaxial layer between the N^+ substrate (conventional epitaxial process) and a diffused P^- region where the anode mosaic contact is placed; see *figure* 0.6. In all these structures the anode is engineered to reduce the injection efficiency and thus obtain the lower stored charge that is required to achieve faster switching.

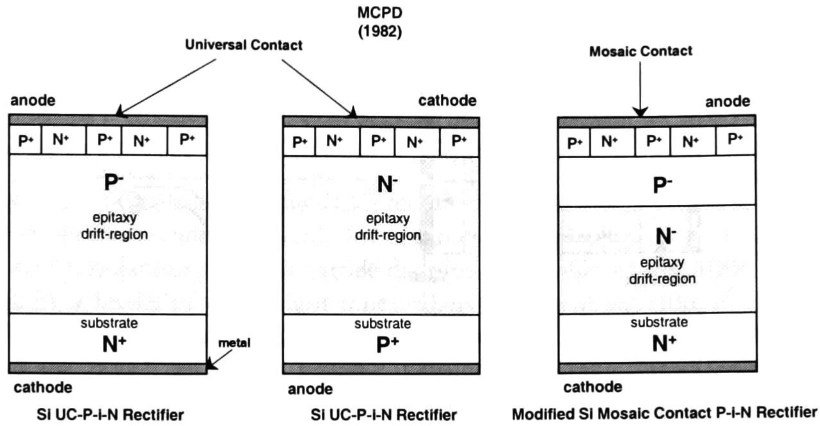


Figure 0.6: *Structures of Low-Loss High-Speed rectifier diodes with a mosaic-type contact.*

Thus, based on conventional process parameters and device structural geometry information from a commercially available power rectifier diode, a detailed numerical analysis of the studied devices was carried out. The technological, electrical and mixed-mode simulations were developed using the advanced two-dimensional device, circuit and system simulator ISE-TCAD's programs. Simulation results are compared to experimental results to verify the benefits that a mosaic-type contact provides compared to a conventional one.

Chapter 1

Power Rectifier Steady-State Physics

This chapter deals with fundamental consideration such as lifetime, with emphasis placed on recombination processes. Different injection levels are considered when a power rectifier diode is forward-biased. A discussion of reverse voltage characteristics is also included. In this section a design criteria for the breakdown voltage will be discussed, as well as the two basic mechanisms responsible for current flow under reverse blocking condition.

1.1. Introduction

AT first glance, it appears that the physics of power semiconductor devices is identical to that of their low power counterpart. Certainly device operation is the same, regardless of physical size. However, under high power operation condition many aspects of device physics take on a efficient sense of importance. The power semiconductor device is exclusively operated in the high current/low voltage ("on") or in the low current/high voltage ("off") regimes, to minimize the losses in the device. Thereby, high power dissipation in the semiconductors only occurs during the switching transients that take the device from the on- to the off-regime and vice versa [21]. Furthermore, certain device structures, such as P-i-N diodes (and P-N-P-N thyristors), have unique advantages for high power applications and are used primarily in these situation alone. In switched mode operation, the power handling capacity of a device is directly related to its ability to support high reverse voltage in the off-state, and to conduct at high forward current levels in on-state.

The reverse breakdown voltage of a junction diode is determined by the resistivity of the P and N regions and by its doping profile. The ability to handle long forward currents necessitates device operation at high levels of injected carriers concentrations, often well in excess the initial concentration of thermally ionized carriers presented in the semiconductor. Thus the background concentration of the semiconductor becomes relatively unimportant in determining the device behavior. Furthermore, the total electron and hole concentration becomes approximately equal in magnitude, so that injection at high levels shares many common characteristics with injection into intrinsic materials. It is appropriate, therefore, to give special considerations to transport phenomena in materials that exhibits intrinsic conduction, specially in lightly doped semiconductors (carrier concentration up $10^{15}cm^{-3}$ in silicon materials) [22].

The P-i-N rectifier was one of the very first semiconductor devices developed for power circuit applications. A P-i-N diode is a P-N junction with a doping profile tailored so that an intrinsic layer, the "*i*-region," is sandwiched between a P layer and an N layer. In practice, however, the idealized i-region is approximated by either a high-resistivity P layer (referred as π, s_P or simply P^-) or a high-resistivity N layer (ν, s_N or N^- layer). On these devices the i-region is flooded whit minority carriers during forward conduction. Due to this, the resistance of the i-region becomes very small during current flow allowing this diodes to carry a high current density during forward conduction. For this reason, the development of P-i-N rectifiers with very high breakdown voltages ranging has been possible. In the following sections, the physics of the steady-state (on-state and off-state) of a P-i-N rectifier is discussed.

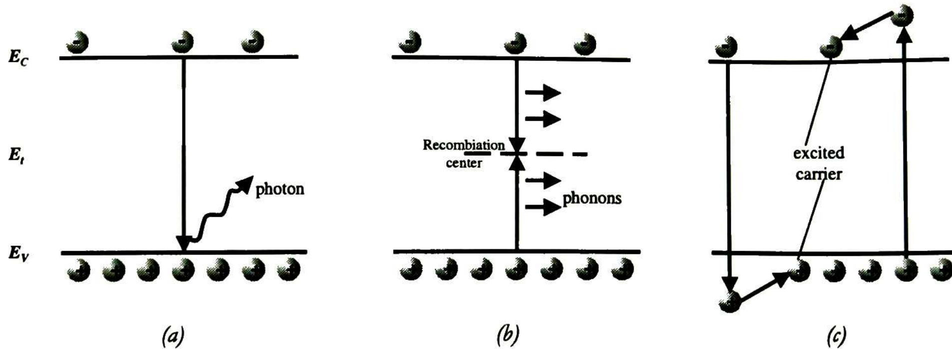


Figure 1.1: *Recombination mechanisms. (a)Radiative. (b)Multi-phonon or Shockley-Read-Hall. (c)Auger.*

1.2. Lifetime

Most semiconductor devices operate under non-equilibrium conditions, e.g., under conditions in which the carrier concentration product pn differs from its equilibrium value n_i^2, where n_i is the intrinsic carrier density. The performance of many semiconductor devices is determined by their tendency to return to equilibrium. Thus, it is essential to tackle an important quantity which characterizes this tendency, *lifetime* (τ). In the case of the injected excess carriers, introduced by light or a forward-biased P-N junction, the mechanism that restores the equilibrium is recombination of injected minority carriers with the majority carriers. Depending on the nature of the recombination process there are three physical mechanisms (see *figure* 1.1) giving rise to the lifetime [14]:

1. *Radiative:* an electron dropping directly from the conduction band into the valence band. The energy of the carriers are dissipated by the emission of a photon, *figure* 1.1(a).
2. *Multi-phonon or Shockley-Read-Hall:* an electron dropping from the conduction band and a hole dropping from the valence band into a recombination center. The energy is dissipated by lattice vibrations or emitted as a phonon, *figure* 1.1(b).
3. *Auger:* electrons from the conduction band and holes from the valence band dropping into surface traps. The energy is given to a third carrier, either an electron or a hole, *figure* 1.1(c).

Radiative recombination dominates in direct bandgap materials like GaAs, multi-phonon is dominant in indirect bandgap semiconductors such as Si, while Auger recombination requires a high density of carriers and therefore dominates under high doping and high injection conditions [23]. Each of the recombination mechanisms of *figure* 1.1 has a generation counterpart. Optical electron-hole pair generation is the counterpart of radiative recombination and impact ionization is that of Auger recombination. The inverse of multi-phonon recombination is the space-charge generation.

1.2.1. Shockley-Read-Hall Recombination Lifetime

During Shockley-Read-Hall (SRH) recombination, electron-hole pairs recombine through deep-level impurities, characterized by the impurity density N_T, energy level E_T in the bandgap, and capture cross sections σ_n and σ_p for electrons and holes, respectively. The four processes which occur in the SRH recombination mechanisms are illustrated in *figure* 1.2. The SRH lifetime is given by [24]

$$\tau = \frac{\tau_p(n_0 + n_1 + \delta n) + \tau_n(p_0 + p_1 + \delta p)}{p_0 + n_0 + \delta n} \tag{1.1}$$

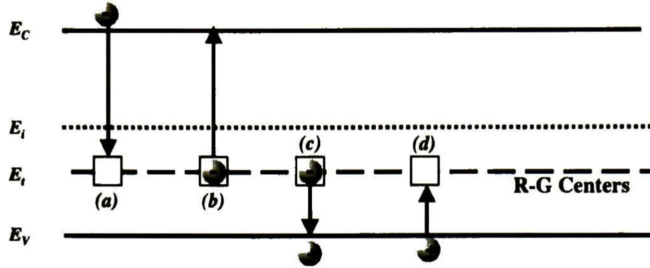


Figure 1.2: *SRH recombination processes: (a)electron capture, (b)electron emission, (c)hole capture, (d)hole emission.*

where p_0 and n_0 are the equilibrium hole and electron densities, δn and δp are the excess carrier densities taken to be equal in the absence of trapping, and n_1 and p_1 are the equilibrium electron and hole densities corresponding to the Fermi-level position E_i in an intrinsic sample, coincident with the recombination level position in the bandgap. This concentrations are given by the expressions [25]

$$n_1 = n_i e^{(E_T - E_i)/kT} \tag{1.2}$$

$$p_1 = n_i e^{-(E_T - E_i)/kT} \tag{1.3}$$

where k is Boltzmann's constant, T the absolute temperature. τ_n and τ_p are the electron and hole minority carrier lifetimes in heavily doped P and N-type silicon defined as [14]

$$\tau_n = 1/\sigma_n \upsilon_{thn} N_T = 1/C_n N_T \tag{1.4}$$

$$\tau_p = 1/\sigma_p \upsilon_{thp} N_T = 1/C_p N_T \tag{1.5}$$

here, υ_{thn} and υ_{thp} are the thermal velocities of electrons and holes, C_n and C_P are the capture rate for electrons and holes, respectively. The SRH theory shows that the rate of the recombination U, in the steady-state through a single-level recombination center is given by [23]

$$U = \frac{\delta n p_0 + \delta p n_0 + \delta n \delta p}{\tau_p (n_0 + \delta n + n_1) + \tau_n (p_0 + \delta p + p_1)} \tag{1.6}$$

Considering a P-type semiconductor, the low-level carrier injection lifetime τ_{ll} holds when the excess minority carrier density δn is small compared to the equilibrium majority carrier density p_0, e.g., $\delta n = \delta p \ll p_0$. For high-level injection $\delta n = \delta p \gg p_0$. Assuming that $\delta n = \delta p$, under conditions of space-charge neutrality and valid when trapping can be neglected, the lifetime can be defined as [14]

$$\tau = \frac{\delta n}{U} = \tau_p \left[\frac{n_0 + n_1 + \delta n}{n_0 + p_0 + \delta n} \right] + \tau_n \left[\frac{p_0 + p_1 + \delta n}{n_0 + p_0 + \delta n} \right] \tag{1.7}$$

Combining equations (1.2) and (1.3), and taking into account that p_0 is much larger than n_0 in the case of a P-type silicon, the equation (1.7) can be written as

$$\tau = \tau_p \left[\frac{\eta}{1+\eta} + \frac{1}{1+\eta} e^{-(2Ei - E_T - E_F)/kT} \right] + \tau_n \left[1 + \frac{1}{1+\eta} e^{-(E_T - E_F)/kT} \right] \tag{1.8}$$

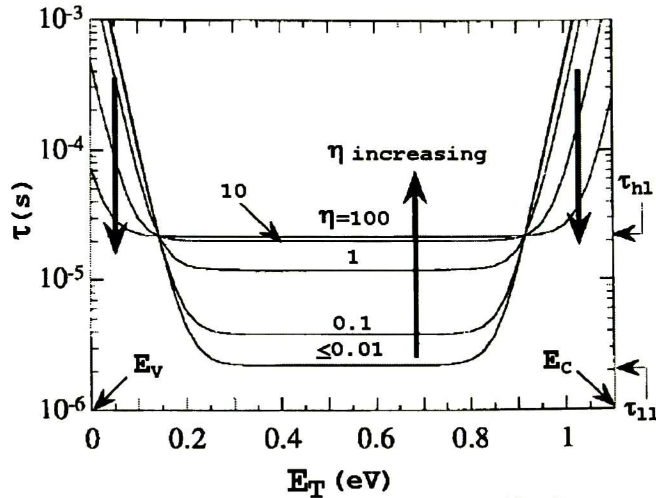


Figure 1.3: *τ versus E_T for N_T=$10^{12}cm^{-3}$, p_O=$10^{16}cm^{-3}$, σ_n=5x$10^{-14}cm^2$, σ_p=5x$10^{-15}cm^2$; the normalized injection level is $\eta=\delta n/p_O$ [25].*

where E_i and E_F are the position of the intrinsic and Fermi energy levels, respectively. *Figure* 1.3 shows τ versus E_T as a function of normalized injection level $\eta=\delta n/p_0$ to show the effect of impurity energy level and injection level on the lifetime. For low-level injection, according to (1.1), the low-level lifetime becomes

$$\tau_{ll} \approx \tau_p\left({n_1}/{p_0}\right)+\tau_n\left(1+{p_1}/{p_0}\right) \tag{1.9}$$

where n_0«n_1 and n_0«p_0. Equation (1.9) is sometimes further approximated as $\tau_{ll}\approx\tau_n$. However, as illustrated in *figure* 1.3 $\tau_{ll}\approx\tau_n$ is valid only for n_1«p_0 and p_1«p_0. The central portion of the curve for $\eta\leq0.01$ is $\tau_n(\eta=\delta n/p_0)$. However, τ increases for impurities with energy levels toward the band edges even at low η. τ also depends on the excess carrier density, as illustrated in *figure* 1.3. If $\delta n=\delta p$»p_0, n_0, p_1, and n_1 (high level injection) then the lifetime becomes

$$\tau_{hl} \approx \tau_n+\tau_p \tag{1.10}$$

Under valid conditions for (1.9) or (1.10), the magnitude of τ for a given energy level and for given capture cross sections always *increases* with injected carrier density. However, as shown in *figure* 1.3, for n_1 or p_1» ($\delta n=\delta p$)»p_0, n_0, the lifetime *decreases* with injection level. The dependence of τ on η is illustrated in *figure* 1.3 by the vertical arrows. This figure clearly shows that τ does not always increase with increasing injection level, as is often stated; e.g., the opposite is true for $E_T\leq0.15$ and $E_T\geq0.9$ in the case shown in *figure* 1.3

Under reverse-bias conditions, where the mobile carriers concentration in the depleted space-charge region can be neglected, equation (1.6) becomes [23]

$$U=-{n_i}/{\tau_{SC}} \tag{1.11}$$

Thus, the space-charge generation lifetime τ_{SC} can be derived from (1.6) for a single-level recombination center as [25]

$$\tau_{SC} = \tau_p e^{\frac{E_T - E_i}{kT}} + \tau_n e^{\frac{-(E_T - E_i)}{kT}} \tag{1.12}$$

τ_{SC} is due to SRH generation and is the only generation lifetime usually considered. Generally, τ_{SC} is higher than τ_n and τ_p, with typically $\tau_{SC} \approx (50\text{-}100)\tau_{n,p}$.

1.2.2. Auger Recombination Lifetime

Auger recombination process becomes significant in heavily doped P- and N-type silicon such as the diffused end regions of power devices. It is also an important effect in determining recombination rates in the lightly doped base regions of power devices operating at high injection levels during forward conduction because of the simultaneous presence of a high concentration of holes and electrons injected into this region. Auger recombination in indirect-gap semiconductors indicate that the process can occur with or without phonon assistance, and may occur directly from band to band or through traps [14]. The transition probability for Auger recombination gives the Auger recombination rate R_A as

$$R_A = C_A \cdot n^2 p \tag{1.13}$$

where C_A is the Auger coefficient, n the electron density in the conduction band, and p the hole density in the valence band. For low-level excitation in the case of heavily doped N-type silicon, the Auger process transfers energy and momentum to an electron to the conduction band and the Auger lifetime is given by [26]

$$\tau_A^N = \frac{\delta p}{R_A} = \frac{p_n - p_{n0}}{C_{An} \cdot n_{n0}^2 (p_n - p_{n0})} = \frac{1}{C_{An} \cdot n_{n0}^2} \tag{1.14}$$

here, p_n and p_{n0} are the minority carrier (holes) and the equilibrium minority-carrier concentration, respectively. Equation (1.14) shows that Auger lifetime varies with the equilibrium majority-carrier (electrons) concentration as $1/(n_{n0})^2$. In the case of P-type silicon, the Auger process occurs by the transfer of energy and momentum to a hole in the valence band and the measured Auger lifetime is given by

$$\tau_A^P = \frac{\delta n}{R_A} = \frac{n_p - n_{p0}}{C_{Ap} \cdot p_{p0}^2 (n_p - n_{p0})} = \frac{1}{C_{Ap} \cdot p_{p0}^2} \tag{1.15}$$

were, n_p and n_{p0} are the minority carrier (electrons) and the equilibrium minority-carrier concentration, respectively. p_{p0} is the majority-carrier (holes) concentration. There are significant uncertainties in the measured and calculated values of the Auger lifetimes and therefore uncertainties in the assigned values of C_A. However, the Auger coefficient tends to be larger for narrow-energy-gap semiconductors. Table 1.1 gives representative values of C_A and τ_A for n_{n0}=2x10^{18}cm^{-3}.

For Auger recombination occurring at high injection levels where the density of electrons and holes is simultaneously large, the Auger lifetime, as measured in heavily excited silicon by laser radiation, is given by [14]

Table 1.1: *Auger recombination coefficients and Auger lifetime for Silicon [26].*

Semiconductor	C_{An} [cm^6/s]	C_{Ap} [cm^6/s]	Lifetime for n_{n0}=2x10^{18}cm^{-3} [s]
N-Type	2.8x10^{-31}		8.9x10^{-7}
P-Type		9.9x10^{-31}	2.5x10^{-6}

$$\tau_A^{\delta n} = \frac{1}{3.4\times 10^{-31}\cdot(\delta n)^2} \tag{1.16}$$

The extremely low Auger lifetimes at high doping concentrations have a strong influence on the injection efficiency and recombination in the end regions of power devices. The Auger lifetime for the case of high injected carrier densities in lightly doped regions is even lower than in the case of heavily doped regions, because the Auger processes requiring two electrons plus a hole and two holes plus an electron can occur simultaneously. At surge current conditions, the injected carrier concentration near the junctions of power devices can exceed 10^{18}cm^{-3}. Since these devices are usually processed to achieve a high Shockley-Read-Hall lifetime (usually in excess of 10μs) the Auger recombination process can play a significant role in affecting current conduction and switching speed at high injection levels. It is important to note that the Auger recombination process occurs simultaneously with the Shockley-Read-Hall recombination process. The effective lifetime is then given by [14]

$$\tau_{eff} = 1/\tau_{SRH} + 1/\tau_A \tag{1.17}$$

where τ_{SRH} is the Shockley-Read-Hall recombination lifetime discussed in section 1.2.1.

1.3. On-State Characteristics

In the case of the P-i-N rectifiers, the injection of minority carriers plays a major role in determining the on-state characteristics. Here, the injection level has a strong influence in the nature of current-voltage (*I-V*) characteristics. Since there is no conceptual difference whether the low doped middle region is nearly intrinsic, P-type or N-type, the attention is focused on the P^+-N^--N^+ structure shown in *figure* 1.4. Thus, from now on the N^--region will be referred as drift-region.

1.3.1. Very Low Level Injection Conditions

For the sake of completeness, the forward conduction analysis starts considering the behavior of the P^+-N^--N^+ structure under very low injection conditions. At very low injection levels, the current flow is dominated by recombination occurring within the space-charge layer of the P-N junction due the presence of deep levels. Each of the carriers generated within the depletion region will be swept out creating a current flow given by [14]

$$J_{SC} = \frac{qn_iW_D}{2\tau_{SC}}\left[e^{\left(V/2V_T\right)} - 1\right] \tag{1.18}$$

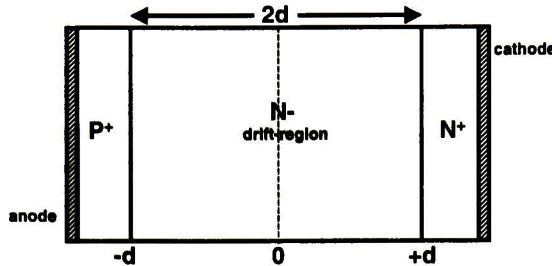


Figure 1.4: *Cross section of a P^+-N^--N^+ rectifier, with W=2d.*

where W_D is the depletion layer, $V_T=kT/q$ the thermal voltage, and V the applied voltage. This form of current dependence upon the forward-bias voltage is observed at very low current levels in P-i-N rectifiers, this is shown in *figure* 1.5 at low values of $q|V|/kT$.

1.3.2. Low Level Injection Conditions

As the applied voltage and forward current increases, holes are injected by the P^+ contact in the drift-region where they are minority and where they recombine. Since the electrons injected by the drift to the P^+ region are negligible, the current across the device is entirely sustained by diffusion of holes in the drift-region where the electric field is zero. The minority carrier distribution in the drift-region is then given by [14]

$$p_N = p_N(0)e^{-(x/L_P)} \tag{1.19}$$

where L_P is the minority carrier diffusion length and $p_N(0)$ is the minority carrier density at the edge of the junction given by

$$p_N(0) = \bar{p}_N e^{(V/V_T)} \tag{1.20}$$

Here, $\bar{p}_N$ is the hole concentration at thermal equilibrium in the drift-region. For an uniformly doped drift-region, the current flow at low injection levels occurs exclusively by diffusion, therefore

$$J = qD_P \left.\frac{dp_N}{dx}\right|_{x=0} = \frac{qD_P\bar{p}_N}{L_P}\left[e^{(V/V_T)} - 1\right] \tag{1.21}$$

where D_P is the diffusion coefficient for holes. The current flow expression under space-charge generation at low injection levels differs in the rate of variation of the current with voltage. *Figure* 1.5 shows how the slope of the *I-V* characteristics changes when the current transport shifts from the generation current dominated regime at very low forward voltage to the diffusion-limited current transport regime under low-level injection conditions. If the width of the drift-region is comparable to the diffusion length and an ohmic contact is assumed at its end (N^--N^+ junction), then the minority carrier density must reduce to zero at this boundary. This distorts the exponential carrier distribution, resulting in a modification of the diffusion current to [27]

$$J = \frac{qD_P n_i^2}{N_D L_P}\tanh\left(\frac{2d}{L_P}\right)\left[e^{(V/V_T)} - 1\right] \tag{1.22}$$

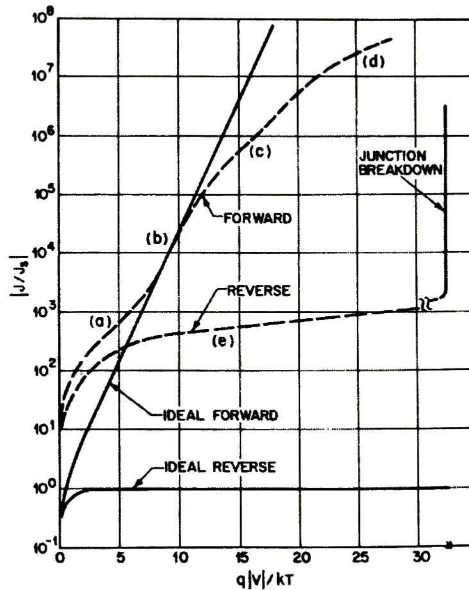


Figure 1.5: *I-V characteristics of a practical Si diode. (a)Generation-recombination current region. (b)Diffusion current region. (c)High-injection region. (d)Series resistance effect. (e)Reverse leakage current due to generation-recombination and surface effect [13].*

where N_D is the donor concentration in the drift-region, d is one half drift-region thickness. Therefore, it follows the same functional dependence as a standard P-N junction, $J_F \propto \exp(V/nV_T)$. n is the ideality factor, equals 2 when the recombination current dominates and equals 1 when the diffusion current dominates.

1.3.3. High Level Injection Conditions

When increasing the applied voltage at a certain point, the injected holes in the drift-region exceed its doping level resulting in a large decrease in the resistance in this region (*conductivity modulation* phenomenon). Hence, *high injection* conditions now hold in the middle region. For neutrality reason, they must equal each other in the middle region; thus, $n(x)=p(x)$>>doping concentration.

Since the recombination predominates, the hole current, coming from the P^+ side is taken over the electrons meeting the holes from the N^+. This takes place not only in the middle region, also in the highly doped regions on both sides, If a SRH recombination is first assumed to occur only in the drift-region, the total current density is given by [28]

$$J = J_m = \int_{-d}^{+d} qU dx = \frac{q}{\tau_a}\int_{-d}^{+d} n(x)dx = \frac{2q\bar{n}d}{\tau_a} \quad (1.23)$$

here, $\tau_a = \tau_{hl}$ is the ambipolar lifetime in the drift-region and $\bar{n}$ is the average drift-region electron/hole concentration. The solution of the continuity equation under steady-state conditions shows that the drift-region carrier distribution is given by [29,30]

$$n(x) = p(x) = \frac{\tau_a J}{2qL_a}\left[\frac{\cosh(x/L_a)}{\sinh(d/L_a)} - B\frac{\sinh(x/L_a)}{\cosh(d/L_a)}\right] \quad (1.24)$$

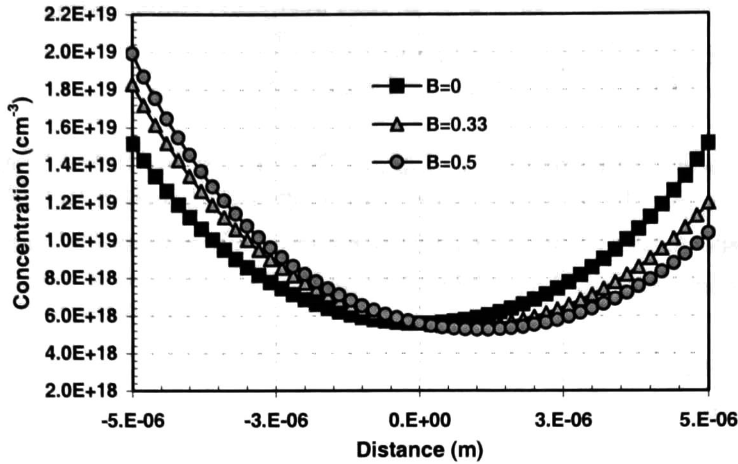


Figure 1.6: *Plot of the distribution in equation (1.24) as a function of the parameter B. Notice that in the case of equal mobilities (B=0) the distribution is symmetrical.*

The ambipolar diffusion length L_a and the ambipolar diffusion constant D_a are given by

$$L_a = \sqrt{D_a \tau_a} \qquad (1.25) \qquad\qquad D_a = 2 \cdot \frac{D_n D_p}{D_n + D_p} \qquad (1.26)$$

where D_n and D_p are the electron and hole diffusion coefficients, respectively. Equation (1.23) shows that increasing τ_a and L_a results in an overall increase in the injected carrier concentration in the base, corresponding to a higher conductivity modulation, thereby reducing the base voltage V_m. The quantity B is a measure for the inequality of mobilities and is given by [27]

$$B = \frac{\mu_n - \mu_p}{\mu_n + \mu_p} = \frac{(\mu_n/\mu_p) - 1}{(\mu_n/\mu_p) + 1} = \frac{b-1}{b+1} \qquad (1.27)$$

where μ_n and μ_p are the electron and hole mobilities, respectively, $b=\mu_n/\mu_p$ is the ratio of carrier mobilities. The distribution in equation (1.24) is illustrated in *figure* 1.6. If the current analysis includes end region recombination, the total current flowing through the rectifier is assumed to consist of the sum of the drift-region and the end region (P^+ and N^+) recombination currents:

$$J = J_m + J_{pN+}(+d) + J_{nP+}(-d) \qquad (1.28)$$

where J_m is the drift-region recombination current given by equation (1.23); $J_{pN+}(+d)$ is the N^+ region recombination current and $J_{nP+}(-d)$ is the P^+ region recombination current. The end region recombination current at the P^+-i interface is given by [31]

$$J_{nP+} = J_{nP+sat} \cdot \left[\frac{n(-d)}{n_{ii}} \right]^2 \qquad (1.29)$$

where

$$J_{nP+sat} = q\frac{D_{nP+}}{L_{nP+}}\coth\left(\frac{d_p}{L_{nP+}}\right)\cdot n_{p0} = q\frac{D_{nP+}}{L_{nP+}}\coth\left(\frac{d_p}{L_{nP+}}\right)\cdot\frac{n_{iP+}^2}{N_A^-} \tag{1.30}$$

here, J_{nP+sat} is the 'saturation current'; D_{nP+}, L_{nP+}, d_p, N_A^-, and n_{p0} are the electron diffusion coefficient, electron diffusion length, the P^+ region length, and the P^+ region doping and electron concentration in the P^+ region, respectively. n_{iP+}^2 is intrinsic carrier concentration in the P^+ region. Similarly, the end region recombination current at the i-N^+ has the form

$$J_{pN+} = J_{pN+sat}\cdot\left[\frac{n(+d)}{n_{ii}}\right]^2 \tag{1.31}$$

where

$$J_{pN+sat} = q\frac{D_{pN+}}{L_{pN+}}\coth\left(\frac{d_n}{L_{pN+}}\right)\cdot p_{n0} = q\frac{D_{pN+}}{L_{pN+}}\coth\left(\frac{d_n}{L_{pN+}}\right)\cdot\frac{n_{iN+}^2}{N_D^+} \tag{1.32}$$

An important deduction that can be made from eqs. (1.29) and (1.31) is that, if the recombination in the middle region is negligible and end region recombination becomes dominant, the injected carrier density in the base will no longer increase linearly with current density but will increase as the square root of the current density. The forward drop will then increase more rapidly with increasing current as observed in the upper portion of *figure* 1.5. Combining equations (1.23) and (1.24), it yields

$$n(x) = p(x) = \bar{n}\frac{d}{L_a}\left[\frac{\cosh(x/L_a)}{\sinh(d/L_a)} - B\frac{\sinh(x/L_a)}{\cosh(d/L_a)}\right] \tag{1.33}$$

Finding $n(-d)$ and $p(+d)$ from this equation and substituting it in equation (1.29) and (1.31) respectively [31]:

$$J_{nP+} = J_{nP+sat}\cdot\left[\bar{n}d/_{n_{ii}L_a}\coth(d/L_a)\right]^2\left[1 + B\tanh^2(d/L_a)\right]^2 = K_n\cdot\bar{n}^2 \tag{1.34}$$

$$J_{pN+} = J_{pN+sat}\cdot\left[\bar{n}d/_{n_{ii}L_a}\coth(d/L_a)\right]^2\left[1 + B\tanh^2(d/L_a)\right]^2 = K_p\cdot\bar{n}^2 \tag{1.35}$$

Substituting equations (1.23), (1.34) and (1.35) into equation (1.28) and solving the resulting quadratic equation for the average drift-region charge [31]:

$$\bar{n} = \frac{qd}{\tau_{hl}(K_n + K_p)}\left[\sqrt{1 + 4J(K_n + K_p)(\tau_{hl}/2qd)^2} - 1\right] \tag{1.36}$$

The total voltage V at the rectifier consists of three components

$$V = V_{P+} + V_m + V_{N+} \tag{1.37}$$

where V_m is the voltage drop in the drift region, V_{P+} and V_{N+} are the voltage drop across the heavily doped regions which can be neglected as long as low level injection exist there.

As shown by Herlet [30] and Hall [32], from the solution of the transport equations along with the carrier continuity equations yields the following relationship between the forward current density J and the applied voltage V across the device

$$J = 2qn_i \cdot \frac{D_a}{d} \cdot F_L \cdot e^{V/2V_T} \tag{1.38a}$$

$$= 2qn_i \cdot \frac{D_a}{d} \cdot F_d \cdot e^{V/2V_T} \tag{1.38b}$$

with

$$F_L = F_d \cdot (d/L_a) = \frac{(d/L_a)\tanh(d/L_a)}{\sqrt{1 - B^2 \tanh^4(d/L_a)}} \cdot e^{-V/2V_T} \tag{1.39}$$

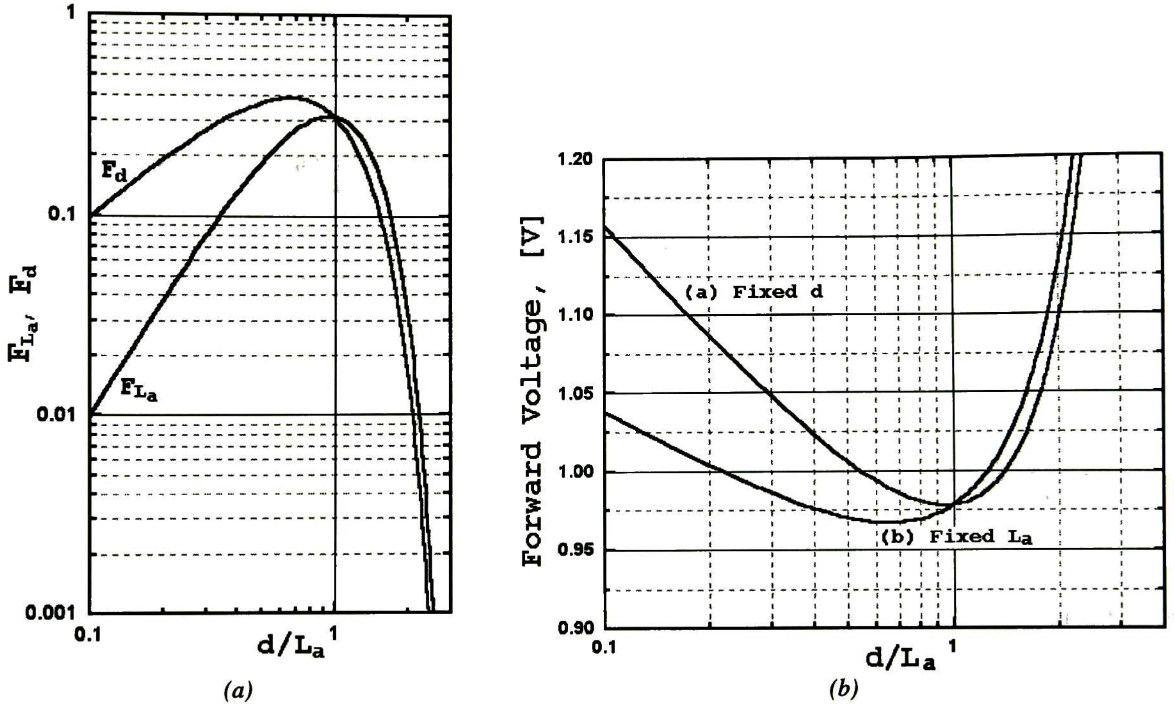
Equation (1.39) claims that the quantity F_L only depends on ratio d/L_a, but not on the load current density J. The voltage drop across the base is given by [33]

$$\frac{V_m}{V_T} = \frac{\frac{8b}{(b+1)^2}\sinh(d/L_a)}{\sqrt{1 - B^2 \tanh^2(d/L_a)}} \arctan\left\{\sinh(d/L_a)\sqrt{1 - B^2 \tanh^2(d/L_a)}\right\} + B \ln\left[\frac{1 + B^2 \tanh^2(d/L_a)}{1 - B^2 \tanh^2(d/L_a)}\right] \tag{1.40}$$

Note that V_m is independent from the injected current J and only depends on the two parameters (d/L_a) and b: high current can ideally be sustained without any increase of the voltage drop. This is the reason for which these structures were used as power rectifiers.

Equation (1.38a) shows that for a given forward current, the effect of a variation in lifetime on the voltage drop is contained in the function F_L, since the remaining parameters in the equation do not involve τ. For the same reason, the effect of a change in d is given by the function F_d in (1.38b). This two functions differ only by the factor (d/L_a). F_L and F_d are plotted in *figure* 1.7(a), it is clear that while they both go through a maximum and are roughly similar for $(d/L_a) \geq 1$, they show a considerable divergence for smaller values of d/L_a, with F_L falling off much more rapidly than F_d. At $(d/L_a)=1$, the two curves coincide as they must, since their difference is due simply to the factor (d/L_a).

The falloff of F_L and F_d for $(d/L_a) \leq 1$ has important consequences, since this is reflected as an increase in voltage drop. The curves (a) and (b) in *figure* 1.7(b) correspond to F_L and F_d, respectively, and from this curves it is appreciated that there exist an optimum value of d and L_a (and hence τ) beyond which any further reduction in d or increase in L_a actually degrades the performance of the device by causing a increase in the forward voltage drop. It is interesting to note that the optimum values for d and L_a do not occur at the same value of (d/L_a).



(a) (b)

Figure 1.7: *(a)The functions F_d y F_{La} plotted against (d/L_a) for silicon where b=3 and B=0.5. (b)The forward voltage drop of a rectifier as a function of (d/L_a). J=280A/cm^2; for curve (a), d=1.5x10^{-2}cm; for curve (b), L_a=1.5x10^{-2}cm.*

The optimum value of L_a for constant d is given by the condition $(d/L_a)\cong1$. However, the optimum value, of d for a constant L_a occurs at $(d/L_a)\cong0.6$. Moreover, the increase in forward drop is more pronounced for increasing L_a than for increasing d. I should be noted that this discussion applies only when the end regions and Auger recombination are neglected. A physical explanation of the behavior of curves (a) and (b) may be given in terms of the relative contributions of the base voltage V_m and the total junction voltage V_j to the overall voltage V. Since the main interest here lies in the effect of carrier lifetime, the following discussion is restricted to curve (a) in *figure* 1.7(b). The derivation of V_j comes from Boltzmann's relations as follows [33]

$$V_j = 2Vt \cdot \ln\left\{\frac{\bar{n}}{n_i}\frac{d}{L_a}\coth(d/L_a)\sqrt{1-B^2\tanh^4(d/L_a)}\right\} \tag{1.41}$$

where the average drift-region electron/hole concentration $\bar{n}$ is related to the current through equation (1.23). In order to support a large carrier concentration at the junction edge, V_j must be raised, as required by (1.41). Increasing the conductivity modulation is, of course, useful as long as V_m forms a significant portion of the applied voltage.

When V_m is small, or is negligible compared to V_j, any further reduction in V_m will offer no advantage; rather, the increase in τ_a will have the adverse effect of increasing V_j and hence V. *Figure* 1.8 shows the plots of V_m and V_j computed from (1.40) and (1.41), respectively. It is clear from the figure that V_m decreases rapidly for decreasing (d/L_a), and reduces to about 1 percent of V_j at (d/L_a)=0.5.

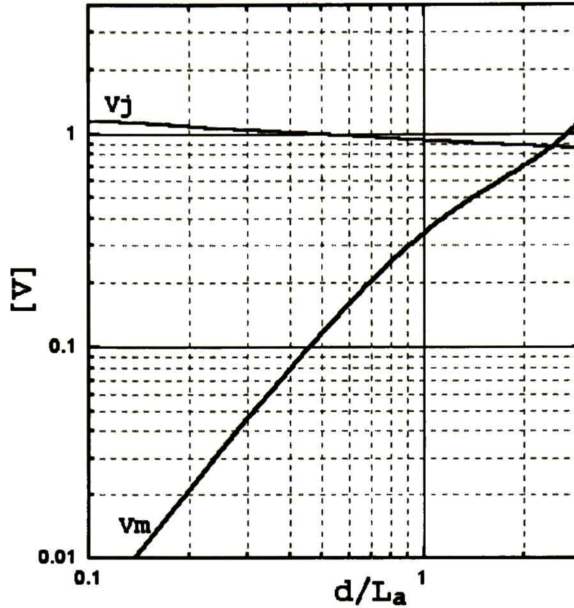


Figure 1.8: *The components of the forward voltage drop given by curve (a) in figure 1.7(a): base voltage V_m and total junction voltage Vj.*

1.3.4. Auger Recombination Effects

Two additional phenomena that affect the current conduction characteristics are carrier-carrier scattering ad Auger recombination. Carrier-carrier scattering occurs in the middle region at high current densities because simultaneous presence of a high concentration of both holes and electrons. The grater probability of this phenomenon causes a reduction in the mobility and diffusion length for both carriers. The reduction in diffusion length with increasing current density produces a decrease in the conductivity modulation in the central portion of the middle region, which, in turn, results in a higher ohmic voltage drop.

At high current densities, the carrier density in the N-base region becomes sufficiently large that Auger recombination begins to affect the carrier statistics. In addition to the SRH recombination, the rate of recombination must include the additional Auger recombination process

$$U = U_{SRH} + U_A = \frac{n(x)}{\tau_{hl}} + C_A[n(x)]^3 \tag{1.42}$$

The inclusion of the Auger recombination term modifies the carrier distribution. To find out the carrier distribution the N-base region in this case, the following continuity equation should be solved

$$D_a \frac{d^2n(x)}{dx^2} = U = \frac{n(x)}{\tau_{hl}} + C_A[n(x)]^3 \tag{1.43}$$

A solution for this differential equation has been obtained [14]

$$n(x) = n_0\left[cn\left(\frac{x-x_0}{L}\middle|m\right)\right]^{-1} \tag{1.44}$$

where $cn(u|m)$ is a Jacobian elliptic function of argument u. In this expression, x_0 is the value of x at which $dn/dx=0$ and $n_0=n(x_0)$. The parameter m and the modified ambipolar diffusion length L_a' are given by

$$m = \frac{\left(C_A\tau_{hl}\,{n_0^2}/{2}\right)+1}{C_A\tau_{hl}n_0^2+1} \tag{1.45}$$

$$L_a' = \sqrt{D_a\tau_{hl}(2m-1)} \tag{1.46}$$

Auger recombination also impacts current transport in the end regions. These regions are doped to very high concentrations, generally exceeding 10^{19}cm^{-3}. Because of the high majority carrier density, Auger recombination alters the minority carrier lifetime. The resulting decrease in the minority carrier diffusion lengths (L_{nP+}, L_{pN+}) increases the recombination current flow (J_{nP+}, here J_{pN+}) into the end regions.

It was previously shown with the aid of *figure* 1.7(b) that, for a fixed base width, the forward drop goes through a minimum when the diffusion length L_a is varied. When end region recombination or carrier-carrier scattering is included in the analysis the forward voltage drop no longer increases rapidly with decreasing diffusion length as shown on the left-hand side of *figure* 1.7(b) at low (d/L_a) values. Instead, the forward voltage drop becomes nearly independent of the lifetime in the N-base region [33].

1.4. Off-state Characteristic

Generally speaking, there are tow variants of power rectifier diodes: (1)the Punch-Through (PT) and (2)the Non-Punch-Through (NPT) diode. The differences between them are that a PT device can be made significantly thinner than an NPT device designed for the same blocking capability. In a PT diode the depletion layer would reach the N^+ region before avalanche breakdown would occur, while higher doping levels on the drift-region would increase the electric filed and result in lower breakdown voltages. PT can be avoided by increasing the doping level or width of the drift-region, but this will reduce the avalanche breakdown voltage, or increase the forward voltage drop respectively.

There are two basic mechanisms responsible for current flow under reverse-bias conditions. The first is associated with the generation of electron-hole pairs within the depletion region, referred to as *space-charge-generation*, and the second is associated with the generation of electron-hole pairs in the neutral regions that diffuse to the junction, referred to as *diffusion leakage current.*

1.4.1. Breakdown Voltage Considerations

Modern high-voltage power semiconductor devices exclusively depend on the P-N junction for rectification. When a reverse-bias is applied to a P-N junction a high-field space-charge region (SCR) appears over the junction. The electric field is dependent on the space-charge concentration according to the well-known Poisson equation in one dimension [13]

$$dE/dx = \left(q/\varepsilon_s\right) \cdot \rho_s, \qquad \text{here} \qquad \rho_s = p - n + N_A^- - N_D^+ \tag{1.47}$$

where E is electric field as a function of x, ε_S the dielectric constant for semiconductor and ρ_S the charge concentration. If the impurity concentration on one side of the junction is much higher than that on the other, breakdown of the junction follows when the maximum electric field, E_{Max}, reaches the critical field strength voltage. The breakdown voltage BV_{P+N} of an abrupt P+-N junction is given by [22]

$$BV_{P^+N} = 60\left[\frac{E_g}{1.1}\right]^{3/2}\left[\frac{N_B}{10^{16}}\right]^{-3/4} \cong 5.34\times10^{13}\cdot N_B^{-3/4} \tag{1.48}$$

where E_g is the energy bandgap for Si and N_B is the N-base doping concentration in cm^{-3}. The depletion layer width W_{SC} at breakdown voltage will extend through the lightly doped region, it is given by [14]

$$W_{SC} = \sqrt{\frac{2\varepsilon_S BV_{P^+N}}{qN_B}} \cong 3.64\times10^3\cdot\left(\frac{BV_{P^+N}}{N_B}\right)^{1/2} \tag{1.49}$$

Using equation (1.49) for N_B=1x10^{14}cm^{-3} the depletion layer width at BV_{P+N}=3000V would be W_{SC}=200µm. This results in an N-base width larger or equal to 200µm, which in forward-bias, the resistive component due to the lightly doping in the base would be an important component, causing a huge voltage drop. As the device thickness is a critical parameter for the performance of the device, the only viable alternative for high-voltage and high-current applications densities is the PT structure (including the P-i-N structure) [21].

Figure 1.9 shows the schematic of electric field distribution for both P+-N and P+-N--N+ (it would be a P+-P--N+) diodes, which varies linearly with distance. Due to the slope of E is proportional to N_B: $(dE/dx)=-\alpha N_B$; generally in the PT case, the doping level of the lightly doped region is lower than that of the NPT. This causes a much slower rate of decrease in the electric field with distance. Since the breakdown voltage is given by the area under the electric field curves in *figure* 1.9, it is clear that the same avalanche breakdown voltage can be obtained for both cases by matching the shaded areas A and B. From *figure* 1.9, the avalanche voltage under the triangle for a NPT diode can be approximated by

$$V_{NPT} \cong \frac{1}{2}E_{Max}W_{SC} \tag{1.50}$$

Similarly, for the PT diode, assuming a trapezoidal shape of the electric field the avalanche voltage V_{PT} can be approximated by [34]

$$V_{PT} = \frac{1}{2}E_{Max}W_{SC} - \frac{1}{2}E_{Max}\frac{W^2}{W_{SC}} = E_{Max}W - \frac{1}{2}E_{Max}\frac{qN_BW^2}{\varepsilon_S} \tag{1.51}$$

where W is the base width.

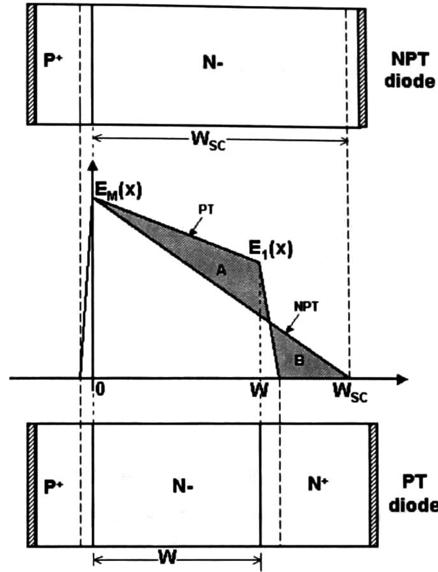


Figure 1.9: *Comparison of Punch-Through diode structure with ideal Non-Punch-Through case.*

The maximum at which the avalanche breakdown occurs can be estimating using [14]

$$E_{Max} = K \cdot N_B^{1/8} \quad \text{and} \tag{1.52}$$

$$K = 4010V \cdot cm^{-5/8} \tag{1.53}$$

where K is an empirical constant. In the case of an epitaxial diode, W becomes the effective width of the drift zone W_{eff}, it can be estimated by the following approximation [35]

$$W_{eff} = THK - 1.65 \cdot X_{jb} \tag{1.54}$$

here, THK is the epitaxial layer thickness and X_{jb} is the anode junction depth. Equation (1.51) is plotted in *figure* 1.10 for several base region widths. It can be seen that the breakdown voltage goes through a maximum when the doping level changes. This is due to a decrease in the critical electric field for breakdown when the doping level decreases. If equation (1.52) is substituted into (1.51), and takes the derivative of equation (1.51) with respect to N_B, it is possible to calculate the optimum value of N_B for a given W that will maximize V_{PT}, this yields

$$N_B = \left(K \cdot \varepsilon_S / 4qW \right)^{8/7} \tag{1.55}$$

Substituting equation (1.52) and (1.55) into (1.51) yields an expression for V_{PT} in terms of the middle layer width

$$V_{PT} = \frac{7}{16} \left(\frac{32 \varepsilon_S K^8 W^6}{q} \right)^{1/7} \tag{1.56}$$

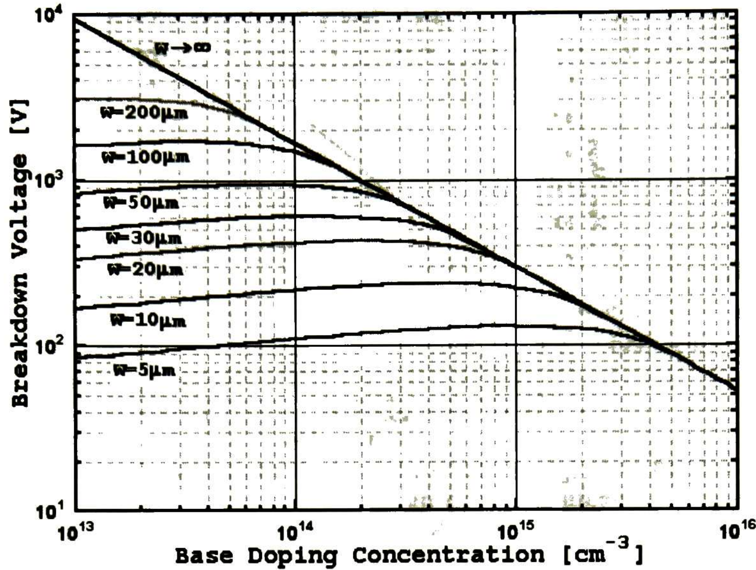


Figure 1.10: *Avalanche breakdown voltage of Punch-Through diodes with several base region widths.*

Punch-through diodes involve a trade-off between doping and width. For a given breakdown voltage, a PT diode has a narrow middle layer, which improves forward conduction, but it also has lighter doping, which can be more difficult to fabricate than a non-punch-through diode. Thus in practice, the optimum value may not be used. The ratio of V_{NPT} and V_{PT} is [34]

$$\kappa = \frac{V_{PT}}{V_{NPT}} = \frac{W\left(2-\left(W/W_{SC}\right)\right)}{W_{SC}} = 2\eta - \eta^2 \tag{1.57}$$

where $\eta = W/W_{SC} < 1$, thus the breakdown voltage of the PT diode is always less than its NPT counterpart, as it can be seen in *figure* 1.11. Finding N_B and W_{SC}, a simple method to design a high-voltage silicon junction rectifier starts from a specified voltage, this will be the extreme case when $V_{PT}=V_{NPT}$. Next, BV and W_{SC} are computed from (1.48) and (1.49), respectively, for N_B lower than that found initially. From now on $BV=V_{NPT}$. Using equation (1.57) or *figure* 1.11 is possible to find η from the rate κ. Now the value of W for the P^+-N^--N^+ structure can be calculated with W_{SC} associated to V_{NPT}. This procedure continues until the optimum W has been found [36]. It is important to note that beyond the optimum point, the base width actually increases slightly at very small values of η.

1.4.2. Space-Charge Generation Leakage Current

Any electron-hole pairs generated within the depletion region of the reverse-bias P-i-N rectifier by thermal energy will be swept out due to the strong electric field. In actual P-N junctions, a finite current flow is always observed. In the case of silicon, which has a large energy gap, the generation current is much larger than the diffusion current at around room temperature. The contribution of the "*leakage*" current from space-charge generation (SCG) can be derived under the assumption of a uniform generation rate U, within the depletion region. Then the leakage current is qU amperes per unit volume of the depletion layer W. From this analysis, the leakage current is given by [7]

$$J_{SC} = {qn_iW}/{\tau_{SC}} \tag{1.58}$$

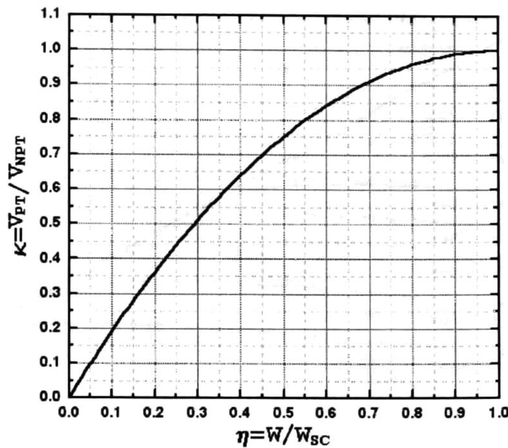


Figure 1.11: *Voltage ratio κ as a function of η.*

The SCG lifetime τ_{SC} is defined by equation (1.12) in section 1.2.1. As discussed earlier, the depletion layer thickness increases with increasing reverse-bias (see equation (1.49)). Consequently, the leakage current due to SCG will increase with increasing the reverse-bias until the depletion layer no longer expands due to PT. J_{SC} is a strong function of temperature, this effect is inherent in (1.58) via the temperature dependence of n_i. However, the SCG current is dominant at lower power device operating temperatures (typically <100°C) because the diffusion current component is an even stronger function of temperature.

1.4.3. Diffusion Leakage Current

Considering the reverse-biased PT diode as that showed in *figure* 1.9, the diffusion current can be calculated from the equation (1.21) for P-N junction current flow under low level conditions by setting V as a negative value. Since the exponential term in the equation then becomes extremely small, the diffusion leakage current is given by [7]

$$J_{DiffN^+} = \left(qD_p n_i^2\right)/\left(N_D L_P\right) \tag{1.59a}$$

where L_p is the diffusion length on the N-side of the junction. A similar expression can be written for the diffusion leakage current due the minority carriers generated in the neutral P-side of the junction as

$$J_{DiffP^+} = \left(qD_n n_i^2\right)/\left(N_A L_n\right) \tag{1.59b}$$

The diffusion leakage current is not a function of the applied reverse-bias except for very small values of the voltage. Furthermore, it can be seen that the diffusion component of the leakage current increases more rapidly with temperature than the space charge generation current because it varies as the n_i^2. As a consequence, the diffusion leakage current becomes dominant in power devices at >100°C. The total reverse leakage current for a P+-N--N+ is then given by [7]

$$J = J_{DiffP^+} + J_{SC} + J_{DiffN^+} = \frac{qD_n n_i^2}{L_n N_A} + \frac{qWn_i}{\tau_{SC}} + \frac{qD_p n_i^2}{L_n N_D} \tag{1.60}$$

This expression can be used to calculate the leakage current for the reverse-biased P-i-N rectifier as a function of bias and temperature. A low leakage current is obtained when the low level lifetime (which determines the diffusion length) is large.

1.5. Summary

In this chapter the main physical models to enhance the possibility of getting analytical solutions to on-state and off-state operation conditions of the silicon P-i-N power rectifiers were presented. Particular emphasis has been devoted on the high injection problems. It has been shown in such structures that the transport mechanism is mostly due to recombination. According to whether the main contribution to recombination is in the drift-region (where high injection occurs) or in the end of regions (where low injection level is still present), different *I-V* characteristics can be found.

The influence of the lifetime variations in the base of the rectifiers in the forward voltage drop has been analyzed. It has been shown that there exist an optimum lifetime value giving a minimum forward voltage, considering the strong dependence upon d/L_a. Increasing lifetime this minimum value can be found. Beyond this optimum value of lifetime (or diffusion length) degrades the performance of the device by causing an increase in the forward voltage drop.

A simple method to estimate the avalanche voltage of a Punch-Through (PT) diode based on its Non-Punch-Through (NPT) diode counterpart was presented, taking into account that the breakdown voltage of the PT diode is always less than the breakdown voltage of the NPT diode with much narrower base region.

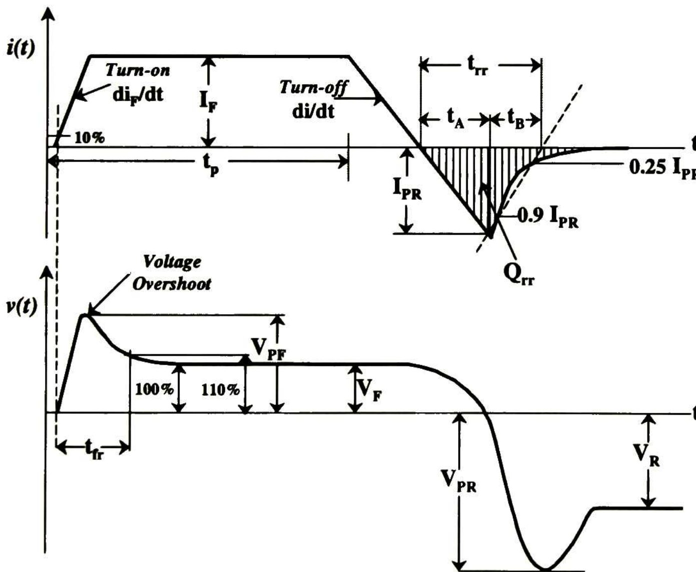
Chapter 2

Power Rectifier Recovery Process

This chapter summarizes the essential switching characteristics of power rectifier diodes so a better understanding of the forward and reverse transient physics can be obtained. The main requirements for the dynamic test and characterization of fast power diodes are discussed, including step and ramp recovery. Finally, analytical solutions of the forward and reverse recovery behavior are presented.

2.1. Introduction

WHEN power rectifiers are used in switching applications, two important drawbacks are worth pointing out. First, when a power rectifier is turned on with a high rate of change di_F/dt, its forward voltage drop has been found to initially exceed its voltage drop during current conduction at the same current level under steady-state conditions. This phenomenon is called *forward voltage overshoot* during turn-on of the rectifier [7]. Under steady-state current conduction, the drift-region resistance is reduced by the injection of the minority carriers. However, during high-speed turn-on, the current may raise much faster than the diffusion of minority carriers injected from the junction. A high voltage drop develops across the drift-region for a short time until the minority carriers can swamp out the drift-region resistance. *Figure* 2.1 shows a typical switching *I-t* and *V-t* waveforms for a power rectifier diode [37].



where

di_F/dt = forward commuting

I_F = forward current

di/dt = reverse commuting

I_{PR} = peak reverse current

V_{PF} = peak forward voltage

V_F = forward voltage

V_R = reverse voltage

V_{PR} = peak reverse voltage

t_{fr} = forward recovery time

t_{rr} = reverse recovery time

$S = t_B/t_A$ = Softness Factor

Q_{rr} = reverse recovery charge

Figure 2.1: *Typical switching I-t and V-t waveforms for a Fast Recovery Epitaxial Diode.*

The level of the voltage overshoot is related to the resistivity and thickness of the drift-region. In general, the drift-region should be designed to minimize its resistance within the constraints to achieve

the target reverse blocking values. A high forward voltage overshoot in the rectifier can be a serious problem in power circuits because this voltage may appear across a switching device (e.g., MOSFET or transistor) used in the circuit and exceed its breakdown voltage, causing a degradation or destruction of the device.

The second and major limitation to the performance of power rectifiers at high frequencies is the losses that occur during switching from the on-state to the off-state. This process is called *reverse recovery* [7]. Such losses are due to the stored charge in the base of the diode. The removal of the stored charge occurs via two phenomena: (1) the flow of a large reverse current (some times referred as sweeping-out current) followed by (2) the recombination of carriers. When the switching frequency of a power circuit increases, the turn-off *di/dt* must be increased, this causes an increase in both the peak reverse recovery current I_{PR}, and the ensuing reverse recovery *di/dt*. If *di/dt* is large, an increase in the breakdown voltage of all the circuit components becomes essential. Raising the breakdown voltage capability causes an increase in the forward voltage drop of power transistors which degrades systems efficiency. Consequently, much of the recent works on power rectifiers have been focused upon improving the reverse recovery characteristics, taking into account an essential trade-off between the switching speed and the forward voltage drop [1, 9, 11, 12, 38].

Power diode structures can be designed to tailor the reverse recovery transient. For instance, power rectifiers are generally designed to minimize the total length of the reverse recovery time, $t_{rr}=t_A+t_B$ (see *figure* 2.1), and increase their associated parameter, $S=t_B/t_A$, which is referred to as the softness factor. The softness is related to the quantity of charges left in the drift-region after the full spread of the depletion zone in blocking mode. To sustain the demand of the current of the external stray inductance, allowing the current to return to zero in a smoother way, the charge left in the drift-region must not be too low. Larger values of S represent a "*softer*" recovery. Recovery softness is particularly important. In fact, when the slope of the recovery (t_B portion) is very fast, it will generate significant radiated and conducted noise. An additional concern is the large voltage overshoot represented by the peak V_{PR}. This voltage overshoot is caused by *di/dt* current flow through inductance in the circuit.

2.2. Power Rectifier Dynamic Test Requirements

Testing the switching characteristics of fast power semiconductor devices is a meticulous process. In order to gain a better understanding of the device and circuit interaction, test circuits with capability of generating various types of current and voltages pulses at different frequencies are necessary to simulate actual electrical stress conditions experienced by typical fast diodes in modern applications. Due to the diode switching performance is largely influenced by external operation conditions, the test circuit should have little impact on the measured results to obtain more accurate diode characteristics and to avoid any misleading results. The test circuit should also enable the user to vary the circuit parameters independently one at a time.

The main forward recovery parameters are the forward recovery time t_{fr}, and the peak forward voltage V_{PF}. The main parameters measured to characterize the diode reverse recovery are the reverse recovery time t_{rr}, reverse recovery charge Q_{rr}, peak reverse current I_{PR}, and the peak reverse voltage V_{PR}. All parameters are mainly dependent on the internal diode structure, but they are also influenced by external factors which govern the circuit operation. These factors include the reverse voltage V_R, forward current I_F, reverse commutating *di/dt*, forward commutating di_F/dt, circuit stray inductance L_C, series resistance R and the junction temperature T_J of the diode. All the switching parameters needed for the characterization of the diode are illustrated in *figure* 2.1. *Figure* 2.2(a) shows an ideal circuit for testing the switching characteristics of fast power diodes.

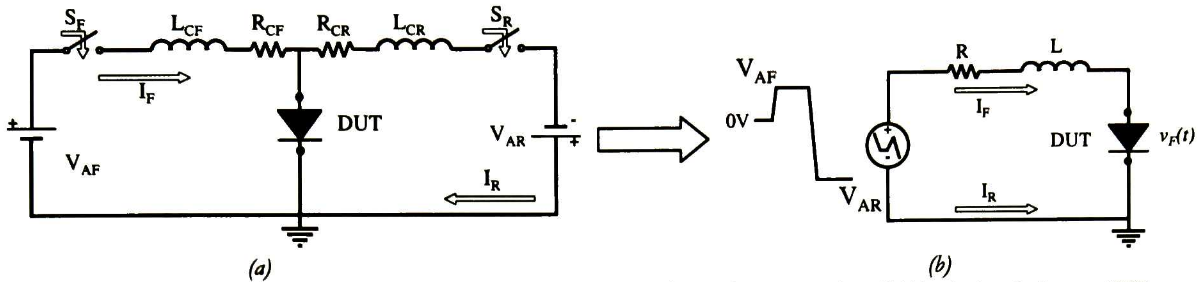


Figure 2.2: *(a)Ideal circuit for testing the power rectifier switching characteristics; (b)ideal circuit fixture [39].*

In order to obtain accurate measurements, the test circuit must allow the following [39]:

1.- The circuit must allow the Device Under Test (DUT) to turn-on in a controllable manner by allowing a known I_F to flow through the diode. The forward commutating di_F/dt is dependent on the applied forward voltage V_{AF} and the forward biasing circuit inductance L_{CF} where

$$\frac{di_F}{dt} = \frac{V_{AF}}{L_{CF}} \tag{2.1}$$

2.- The circuit must allow I_F to flow through the DUT for a sufficient period of time t_p. This will enable the diode to reach its stable conduction sate, without increasing the diode's temperature due to self heating effects.

3.- The circuit must allow the current to be removed from the DUT in a controllable manner. For low values of R_{CR}, the commuting di/dt is mainly dependent on the applied reverse voltage V_{AR} and the reverse circuit inductance L_{CR}, which always supports the reverse voltage instantly at turn-off. The reverse commuting di/dt is given as

$$\frac{di}{dt} = -\frac{V_{AR}}{L_{CR}} \tag{2.2}$$

4.- The circuit must allow V_{AR} to appear across the DUT at the end of the reverse recovery period. At this point the full blocking state is established across the diode P-N junction.

Figure 2.2(b) shows an ideal circuit fixture, where both resistance and inductance for the forward and reverse bias circuits are assumed equal. For the sake of numerical convergence, this circuit configuration is useful when a mixed-mode simulation tool is used. The circuit retains the essential features of inductive switching (*ramped reverse recovery*). By the simulation approach, the applied voltage is set by a time dependent voltage source through a piecewise linear function.

When the circuit showed in *figure* 2.2(b) is purely resistive (*step reverse recovery*), immediately after V_{AF} goes to V_{AR}, the reverse current I_R might be comparable in magnitude to the forward current if $V_{AR}/R \sim V_{AF}/R$. Subsequently, the current through the diode remains essentially constant at $-I_R$ for a limited period of time before eventually decaying to the steady-state value. The period of time during which the reverse current remains constant is known as the *storage time* or *storage delay time*, t_S; while t_{rr} is the total time required for the reverse current to decay to 10% of its maximum magnitude. The recovery time t_r is the difference between t_{rr} and t_S. The cited times characterizing the transient are also defined graphically in the waveforms shown in *figure* 2.3(a).

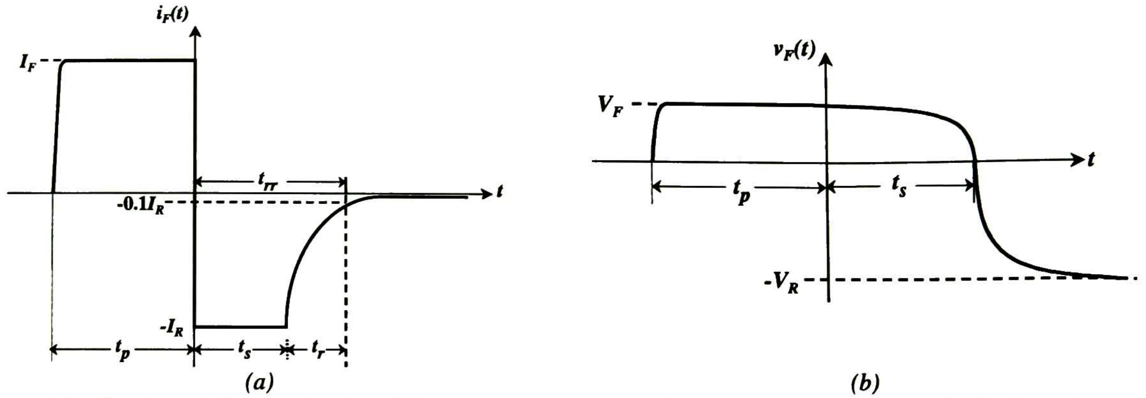


Figure 2.3: *Sketch and characterization of the step reverse recovery. (a)current-time transient and (b)voltage-time transient.*

The variation of the instantaneous diode voltage v_F, corresponding to the *I-t* transient is shown in *figure* 2.3(b). It can be noticed from the figure that (i)the junction remains forward-biased for $0<t<t_S$ even though the externally applied voltage is such as to reverse-bias the diode, and (ii)the $t=t_S$ point correlates with $v_F=0$. In analyzing the transient response, the assumption that the voltages V_{AF} and V_{AR} are large compared to the maximum forward voltage drop V_F across the diode is made. Under the stated assumption

$$I_F = \frac{V_{AF} - V_F}{R} \cong \frac{V_{AF}}{R}. \qquad \text{for } V_F < V_{AF} \tag{2.3}$$

and

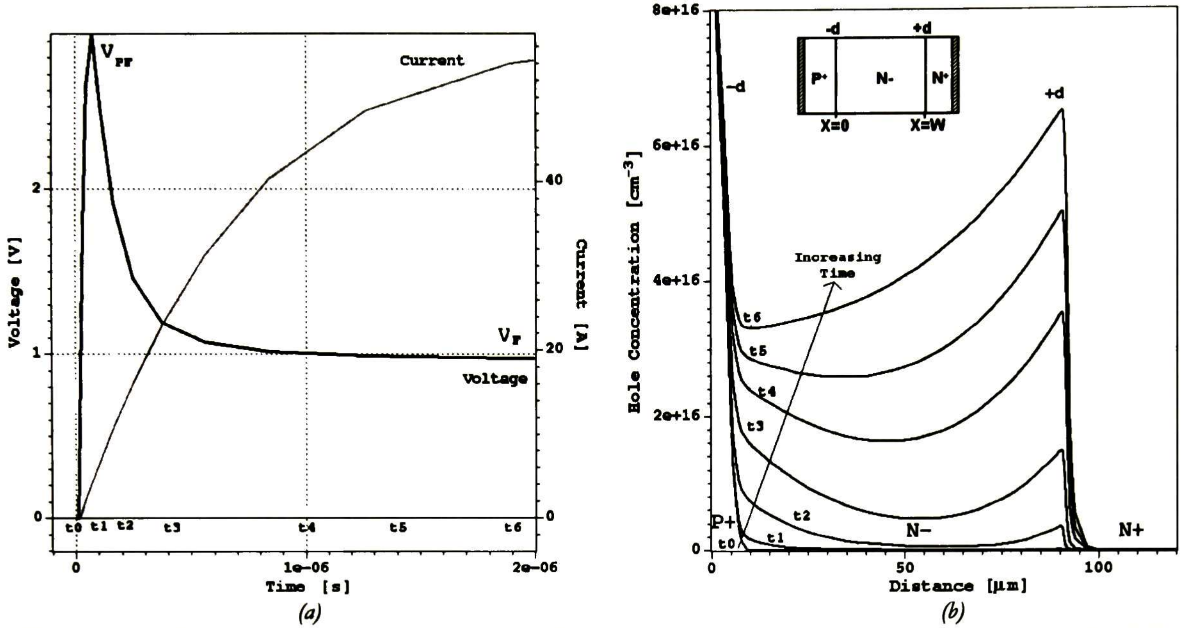
$$I_R = \frac{V_{AR} + v_F\big|_{0<t\leq t_s}}{R} \cong \frac{V_{AR}}{R} \qquad \text{for } |v_F(t)| << V_{AR} \tag{2.4}$$

It is necessary to point out that it is possible to make I_R larger than I_F (e.g., increasing V_{AR}), which increases the rate at which the stored is removed by the reverse current flow. The storage time t_s as defined in *figure* 2.3(a) is directly proportional to the average lifetime of the charge carriers in the device, τ, by [40]

$$t_s = \tau \left[erf^{-1}\left(1 + \frac{1}{I_R / I_F} \right) \right]^2 \tag{2.5}$$

This formula is based on the charge control model. It should be noted that τ is a complex function of parameters, such as the diode structure, carrier lifetimes, and carrier density, so it is an "effective" lifetime.

The difference between inductive switching and resistive switching is the fact that under resistive switching, reverse current is constant during the initial phase, whereas during inductive switching the reverse current trough the diode falls off at the rate determined by the external circuit. From now on the rest of this chapter will extensively treat the inductive switching unless otherwise specified.



(a) (b)

Figure 2.4: *(a)Forward recovery characteristics and (b)evolution of associated excess minority carriers in the drift-region during forward recovery.*

2.3. Forward (turn-on) Transient

Forward switching characteristics are seldom specified on rectifier data sheets even though a diode's turn-on behavior is important in a number of power electronic applications operating at high frequencies. The importance of having fast turn-on and low dynamic impedance is eventually not fully appreciated [41]. This section outlines the principles of the minority carrier distribution profile and its effect on the forward recovery behavior.

Typical diode current and voltage waveforms obtained from simulation using ISE-TCAD software during forward recovery are shown in *figure* 2.4(a). The growth of the stored N drift-region hole charge with time is pictured in *figure* 2.4(b). During the turn-on portion of the diode waveforms (encompassed by the times labeled from t_0 to t_6 in *figure* 2.4(b)) two physical processes occur in sequence. First, when the depletion layer is in its thermal equilibrium level, the P-N junction becomes forward-biased and the injection of excess carriers across the junction into the drift-region limits commences at time t_1, thus marking the start of a second phase. During the second phase, the excess carries distribution in the drift-region grows toward the steady-state value that can be supported by the forward diode current I_F (see *figure* 2.4(b)). Notice that in the P-i-N diode, the P-i (e.g., P^+-N^-) junction is forward-biased while the electron barrier height at the i-N (e.g., N^--N^+) junction is reduced. As a result, holes from P-side and electrons from N-side can be injected into the drift-region modulating its conductivity.

A simple interpretation of this sequence of events would lead to expect that the diode's voltage would rise smoothly and monotonically from its initial value, zero voltage bias, to a steady-state forward-bias value. During this phase, the diode exhibits turn-on transients (forward recovery) due to "*conductivity modulation lag*" effect. This effect arises because it takes a finite amount of time for the charge profile to change in the drift-region of the device. Thus, the charge profile in the drift-region will always lag the diode current vector (capacitive effect). When the diode is turned-on, because of the low dopant density in the drift-region, a very high electric field is set up in the drift-region to allow the flow of

current (current is determined by the external circuit conditions). As a result of this high electric field, there is a significant voltage drop across the drift-region during this operation phase. Thus, during turn-on transients, for a given current density, there is a significant higher electric field and lower carrier concentration in the drift-region compared to the steady-state.

It has been shown that during turn-on transient, the voltage across the diode is dominated by the voltage drop in the drift-region V_m, as opposed to steady-state when V_m is a negligible portion of the total voltage drop [42]. The growth of the diode voltage slows and eventually turns over as the drift-region becomes shorted out by the large amount of carrier injection into it. In addition, the inductive contribution ends when the diode current stabilizes at I_F. The interval during which the voltage falls from the peak overshoot value to the steady-state forward value ($t_{fr} \cong t_4$) marks the completion of the transient growth of the excess charge distribution in the drift-region.

In [43] it has been shown that is possible to obtain an analytical solution of the forward transient for P^+-N^--N^+ or P^+-P^--N^- structures based on the case of P^+-i-N^+ structure. If the forward current density J_F, in a P^+-N^--N^+ diode is sufficiently large, the injected carriers will overwhelm the background doping, allowing the analytical results for a P^+-i-N^+ diode to be used to determine the transient response. Assuming that quasi-neutrality exists in the lightly doped n-type middle layer. Then

$$p = n - N_D \tag{2.6}$$

where n and p are the densities of free electrons and holes, respectively; N_D is the donor impurity density. Also assume that that the doping in the P^+ and N^+ regions is much higher than in the N^- middle region. Then the current at the P^+-N^- junction (x=0, see insert of *figure* 2.4(b)) will be almost entirely a hole current, and the current at the N^--N^+ junction ($x=W$) will be an electron current:

$J_p(0,t) = J_F$; (2.7) $J_n(0,t) = 0$; (2.8) $J_p(W,t) = 0$; (2.9) $J_n(W,t) = J_F$; (2.10)

here, W is the lightly doped middle layer width. The transport equations can be written as [29]

$$J_p(x,t) = q\mu_p\left(-V_T\frac{\partial p(x,t)}{\partial x} + p(x,t)E(x,t)\right) \tag{2.11a}$$

and

$$J_n(x,t) = q\mu_n\left(V_T\frac{\partial n(x,t)}{\partial x} + n(x,t)E(x,t)\right) \tag{2.11b}$$

where E is the electric field strength, $V_T=kT/q$ the thermal voltage, μ_n and μ_p are electron and hole mobilities, respectively. Using equations (2.6) to (2.10) allows the current at either junction to be calculated in terms of doping and carrier distribution as [43]

$$J_F = -q\mu_n V_T\left(2 - \frac{N_D}{n(0,t)}\right)\frac{\partial n(0,t)}{\partial x} \tag{2.12a}$$

and

$$J_F = q\mu_n V_T\left(1 + \frac{n(W,t)}{n(W,t) - N_D}\right)\frac{\partial n(W,t)}{\partial x} \tag{2.12b}$$

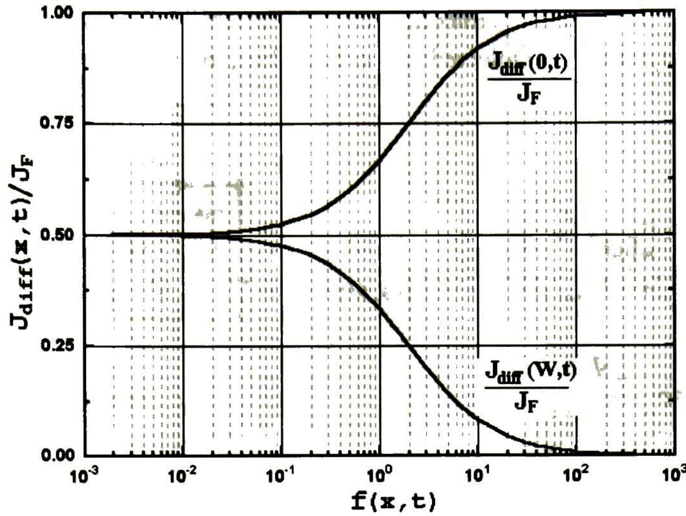


Figure 2.5: *Diffusion current as a fraction of the total current, at both junctions.*

identifying the first term in equations (2.11a) and (2.11b) as the diffusion term J_{diff}, and defining [43]

$$f(x,t)=\frac{N_D}{n(x,t)-N_D} \tag{2.13}$$

Equations (2.12a) and (2.12b) can be rewritten as [43]

$$\frac{J_{diff}(0,t)}{J_F}=\frac{1}{2-\frac{f(0,t)}{f(0,t)+1}} \tag{2.14a}$$

and

$$\frac{J_{diff}(W,t)}{J_F}=\frac{1}{2+f(W,t)} \tag{2.14b}$$

Equations (2.14a) and (2.14b) show that the balance of the drift and diffusion currents at the junctions is affected by the doping in the middle layer. These two functions are plotted as a function of f in *figure* 2.5. In the limiting case of no middle layer doping, $N_D \to 0$, and hence, $f \to 0$, both functions approach the value 0.5. In other words, the drift and diffusion currents at both junctions in a P^+-i-N^+ diode are equal. This remains largely true for $f<0.1$. As N_D increases, and f increases correspondingly, the current at the N^--N^+ junction is dominated by a drift current, and the current at the P^+-N^- junction is dominated by the diffusion component. Since the diffusion current at the high-low junction becomes small, dn/dx is also small and very little charge is built up at the high-low junction. At the early time, immediately after the beginning of the forward transient current pulse, no holes will have yet traveled to the N^--N^+ junction, so it is possible to write [43]

$$\frac{E_{bulk}}{dx}=\frac{q}{\varepsilon_S}\left(n\left(W,0^+\right)-N_D\right) \tag{2.15}$$

where ε_S is the dielectric constant for semiconductor. The current in the bulk of the middle layer must be ohmic, since little charge has been injected and $n \approx N_D$. Thus, in this region

$$E_{bulk} = \frac{J_F}{q\mu_n N_D} \tag{2.16}$$

If this bulk electric field is assumed to build up from zero over a short distance Δx near the N^--N^+ junction, then $dE/dx \approx E_{bulk}/\Delta x$. Combining equations (2.15), (2.16), and (2.13) yields [43]

$$f(W,0^+) = \frac{N_D}{n(W,0^+) - N_D} \approx \frac{q^2 N_D^2 \mu_n \Delta x}{\varepsilon_S J_F} \tag{2.17}$$

An estimate for Δx can be obtained by writing [43]

$$\frac{E_{bulk}}{\Delta x} = \frac{q}{\varepsilon_S}\left(n\left(W,0^+\right) - N_D\right) \approx \frac{q}{\varepsilon_S}\left[\left(N_D + \frac{dn}{dx}\Delta x - N_D\right)\right] = \frac{q}{\varepsilon_S}\frac{dn}{dx}\Delta x \tag{2.18}$$

dn/dx can be estimated from the electron diffusion current. Of course, the diffusion current to total current ratio varies with f, as discussed above. Since the diode behaviors for $f>>1$ and $f<<1$ are quite different, the most interesting case is for $f=1$, where the diffusion current is 1/3 of J_F. This case is a "critical" boundary case. Thus [43]

$$\frac{dn}{dx} = \frac{J_F}{3q\mu_n V_T} \tag{2.19}$$

Combining equations (2.16) to (2.19) to eliminate Δx yields

$$f\left(W,0^+\right) = J_0/J_F \tag{2.20}$$

where [43]

$$J_0 = \sqrt{\frac{3\mu_n^2 V_T}{\varepsilon_S}\left(qN_D\right)^3} \tag{2.21}$$

Hence, for current densities substantially larger than J_0 (e.g., $J_F>10J_0$), the diode acts as though it were intrinsic, leading to balanced drift and diffusion currents, and charge injection from both junctions. For current densities substantially less than J_0 (e.g., $J_F<0.1J_0$), the charge injection will be dominated by the P^+-N^- junction, and relatively little charge will be stored at the high-low junction. Since $J_0 \propto N_D^{3/2}$, the critical current density $J_F=J_0$ (corresponding to $f=1$) increases moderately quickly with increasing doping, and the usefulness of the intrinsic approximation becomes restricted for even relatively light doping levels.

Physically, (2.13) shows that the condition $f(x,t)=1$ corresponds to an injected carrier density of $n(x,t)=2N_D$. Thus, if the forward current is large enough such that $n(W,0^+)>>2N_D$ at the high–low junction immediately after the beginning of the transient (e.g., $J_F>>J_0$) the diode will act as a P-i-N

Test Circuits and Waveforms

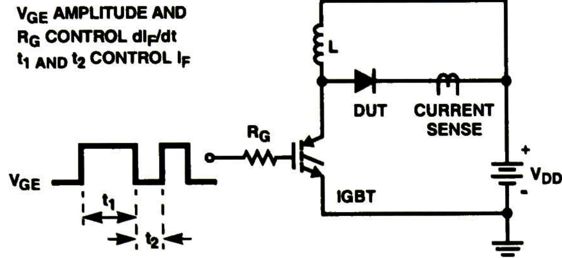


FIGURE 8. t_{rr} TEST CIRCUIT

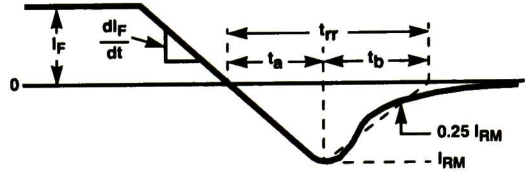


FIGURE 9. t_{rr} WAVEFORMS AND DEFINITIONS

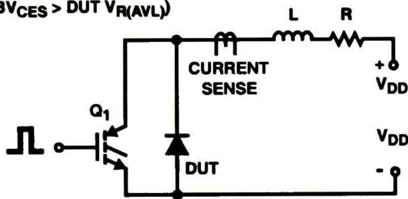


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

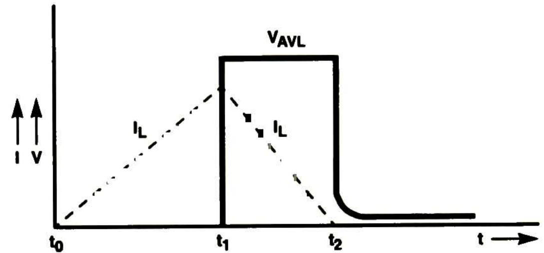


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

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Typical Performance Curves (Continued)

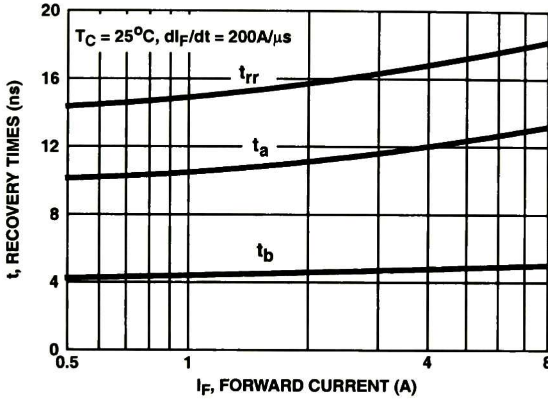

FIGURE 3. t_{rr}, t_a AND t_b CURVES vs FORWARD CURRENT

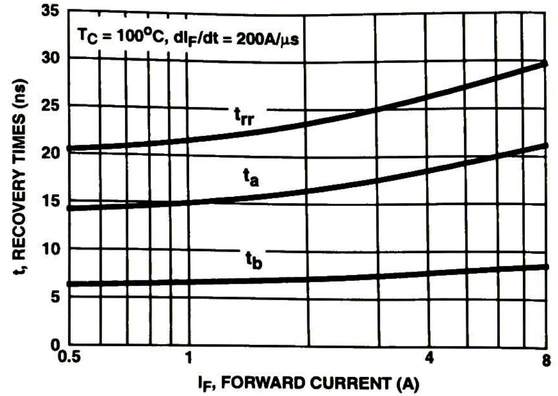

FIGURE 4. t_{rr}, t_a AND t_b CURVES vs FORWARD CURRENT

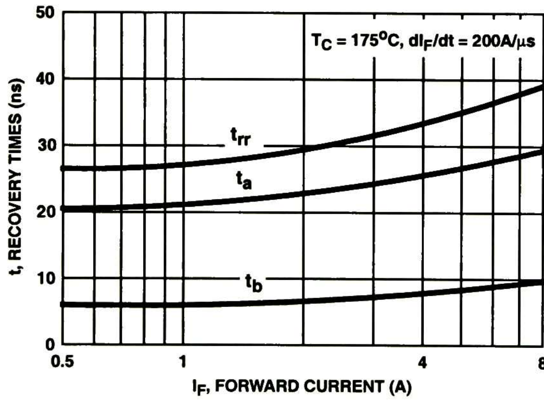

FIGURE 5. t_{rr}, t_a AND t_b CURVES vs FORWARD CURRENT

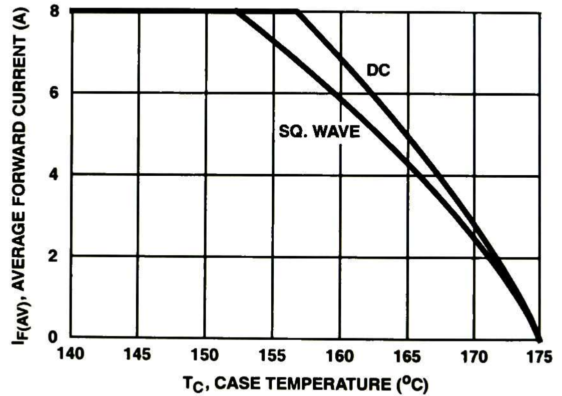

FIGURE 6. CURRENT DERATING CURVE

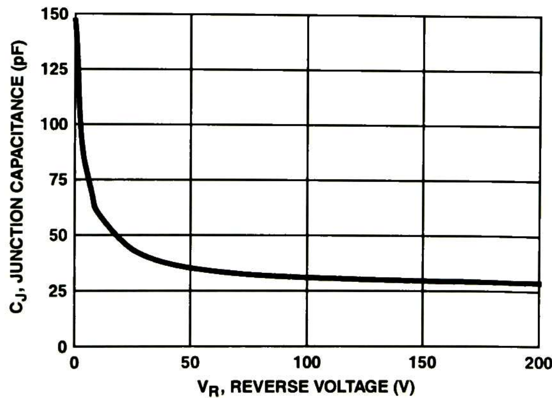

FIGURE 7. JUNCTION CAPACITANCE vs REVERSE VOLTAGE

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Electrical Specifications T_C = 25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
V_F	I_F = 8A			0.975	V
	I_F = 8A, T_C = 150°C			0.895	V
I_R	V_R = 200V			100	μA
	V_R = 200V, T_C = 150°C			500	μA
t_{rr}	I_F = 1A, dI_F/dt = 200A/μs			25	ns
	I_F = 8A, dI_F/dt = 200A/μs			30	ns
t_a	I_F = 8A, dI_F/dt = 200A/μs		13		ns
t_b	I_F = 8A, dI_F/dt = 200A/μs		5		ns
Q_{RR}	I_F = 8A, dI_F/dt = 200A/μs		25		nC
C_J	V_R = 10V, I_F = 0A		60		pF
$R_{\theta JC}$				3	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).

I_R = Instantaneous reverse current.

t_{rr} = Reverse recovery time (See Figure 9), summation of $t_a + t_b$.

t_a = Time to reach peak reverse current (See Figure 9).

t_b = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 9).

Q_{RR} = Reverse recovery charge.

C_J = Junction Capacitance.

$R_{\theta JC}$ = Thermal resistance junction to case.

pw = Pulse width.

D = Duty cycle.

Typical Performance Curves

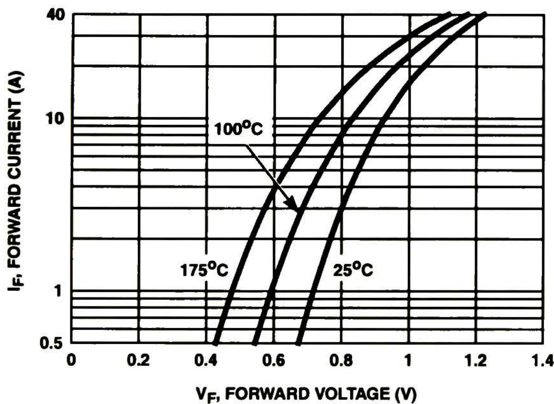

FIGURE 1. FORWARD CURRENT vs FORWARD VOLTAGE

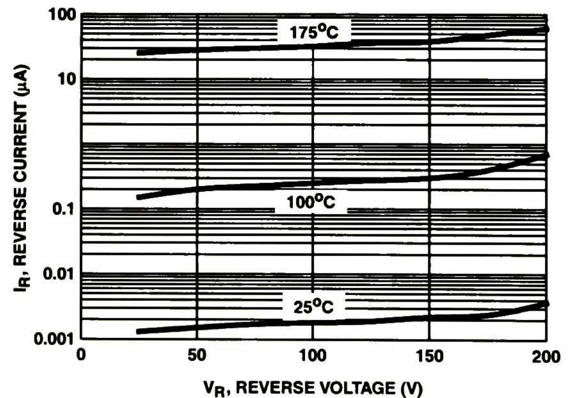

FIGURE 2. REVERSE CURRENT vs REVERSE VOLTAGE

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MUR820, RURP820

Data Sheet | January 2000 | File Number 1355.5

8A, 200V Ultrafast Diodes

MUR820 and RURP820 are ultrafast diodes with soft recovery characteristics (t_{rr} < 25ns). They have low forward voltage drop and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

Formerly developmental type TA09223.

Ordering Information

PART NUMBER	PACKAGE	BRAND
MUR820	TO-220AC	MUR820
RURP820	TO-220AC	RURP820

NOTE: When ordering, use the entire part number.

Symbol

Features

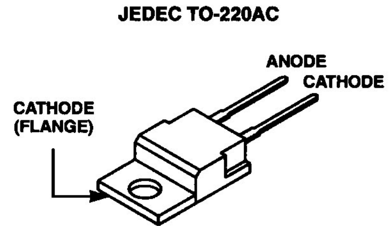
- Ultrafast with Soft Recovery . . . . <25ns
- Operating Temperature. . . . . .175°C
- Reverse Voltage 200V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Packaging

JEDEC TO-220AC



Absolute Maximum Ratings T_C = 25°C, Unless Otherwise Specified

		MUR820 RURP820	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	200	V
Working Peak Reverse Voltage	V_{RWM}	200	V
DC Blocking Voltage	V_R	200	V
Average Rectified Forward Current (T_C = 157°C)	$I_{F(AV)}$	8	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FRM}	16	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	100	A
Maximum Power Dissipation	P_D	50	W
Avalanche Energy (See Figures 10 and 11)	E_{AVL}	20	mJ
Operating and Storage Temperature	T_{STG}, T_J	-65 to 175	°C

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Appendix C

List of Publications

1. H.E. Aldrete-Vidrio, J. Santana, and J.L. del Valle "Technological, Electrical and Mixed-Mode Simulation of Fast Recovery Epitaxial Diodes (FREDs) Using a P^+/N^+ Mosaic Contact," to be presented at *8th International Workshop Ibechip* 2002, 3-5 April 2002, Guadalajara, México.

2. P. Garcia, J.L. del Valle, Y. Matsumoto, K. Akinade and H.E. Aldrete-Vidrio, "The Use of T-CAD Tool for Yield Improvement on Fast Switching Power Rectifiers," to be presented at *4th International Caracas Conference on Devices, Circuits and Systems –ICCDCS–*, 17-19 April 2002, Seaport Conference Center, ARUBA.

3. H.E. Aldrete-Vidrio, J. Santana, and J.L. del Valle, "Stored Charge Control of P-i-N Diodes: A Simulation Approach," to be presented at *4th IEEE International Caracas Conference on Devices, Circuits and Systems –ICCDCS–*, 17-19 April 2002, Seaport Conference Center, ARUBA.

4) *Switching behavior mixed-mode "transient_des.cmd"*

```
*********************************************************************
#  DIODE -->  "Switching Behavior Characteristics"
*********************************************************************
Plot
{
   Doping DonorConcentration AcceptorConcentration eDensity/vector
   hDensity/vector
   Current/vector eCurrent/vector hCurrent/vector
   ConductionCurrent/Vector DisplacementCurrent/Vector
   SRHRecombination AugerRecombination TotalRecombination
   AvalancheGeneration eAvalanche hAvalanche
   eLifetime hLifetime eMobility hMobility SpaceCharge Potential
}
Physics
{
Mobility(DopingDependence HighFieldSaturation NormalElectricField
        CarrierCarrierScattering)
Recombination (SRH (DopingDep ExpTempDependence) Auger
               Avalanche(VanOverstraeten Eparallel))
EffectiveIntrinsicDensity(Slotboom)
Temperature=298
}

Math
{
        RelErrControl
        Derivatives
        AvalDerivatives
        NoAutomaticCircuitContact
}

File
{
        Output="@log@"
}
Dessis diode{
Electrode
        {
          { Name="anode"     Voltage=0.0  AreaFactor=24.833e3}
          { Name="substrate" Voltage= 0.0 AreaFactor=24.833e3}
        }
File
        {
        Grid      "@grid@"            #input
        Doping    "@doping@"          #input
        Param      "dessis50ns"
        }
System{
        diode pin(anode=node2 substrate=0){
                File
                {
                Current    "@plot@"
                Plot       "@dat@"
                }
        }
        r r1    (node1 node3) {r=@RESISTOR@}
        v v1    (node1 0)     {type="pwl" pwlfile="switch.pwl"}
        llin l1 (node3 node2) {ind=@INDUCTOR@}
        plot "n@node@_circ.plt" (
        time() node1 node2 node3 i(r1 node3) i(pin 0) i(l1 node2)
        )
initialize (node1=0)
}

Solve
{
Coupled (method=blocked)
        {circuit}
Plugin (Iterations=0 BreakOnFailure)
        {Poisson Hole Electron Circuit Contact}

Coupled(iterations=30 Digits=4)
        {Poisson Hole Electron Circuit Contact}
Transient(
        InitialStep=1.0e-15 MaxStep=1e-6 MinStep=1e-15
        InitialTime=0 FinalTime=3.5e-6
        Increment=1.5 Decrement=2.0
        )
        {
        coupled(Iterations=20 Digits=5)
                {Poisson Hole Electron Circuit Contact}
        }
}
```

5) *Time dependent voltage source "switch.pwl"*

```
0          0
0.50e-6    0
0.52e-6     30
10.00e-6    30
10.02e-6   -28.80
12.00e-6   -28.80
```

```
  hDensity/vector ElectricField/vector eEnormal hEnormal
  eEffectiveField eEffectiveField eEparallel hEparallel
  Current/vector eCurrent/vector hCurrent/vector
  ConductionCurrent/Vector DisplacementCurrent/Vector
  SRHRecombination AugerRecombination TotalRecombination
  AvalancheGeneration eAvalanche hAvalanche Potential eQuasiFermi
  hQuasiFermi eGradQuasiFermi hGradQuasiFermi IntrinsicDensity
  EffectiveIntrinsicDensity BandGap BandGapNarrowing
  ConductionBandEnergy ValenceBandEnergy LatticeTemperature
  eLifetime hLifetime eMobility hMobility SpaceCharge
}

Math
{
        Derivatives
        AvalDerivatives
}

Solve
{
        *initial solution
Plugin (Iterations=0 BreakOnFailure)
        {Poisson Hole Electron}
Coupled(Digits=50)
        {Poisson Hole Electron}
*ramp anode from 0 to 2V in steps of 0.015V
QuasiStationary(
        InitialStep=7.5e-3 MaxStep=7.5e-3
        Goal { name="anode" voltage=2 })
        {
        coupled(Iterations=20 Digits=100)
                {Poisson Hole Electron}
        plot ( FilePrefix="5u_1V" Time= (0.5) NoOverwrite )
        }
}
```

3) *Reverse Steady-State Characteristic "revesre des.cmd"*

```
*********************************************************************
# DIODE --> "I-V Reverse Static Characteristics
*********************************************************************
Electrode
{  { Name="anode"     Voltage=0.0 AreaFactor=24.833e3 }
   { Name="substrate" Voltage=0.0 AreaFactor=24.833e3  Resistor
1e10}
}

File {
        Grid        "@grid@"
        Doping      "@doping@"
        Current     "@plot@"
        Output      "@log@"
        Plot        "@dat@"
        Param       "dessis50ns"
}

Physics
{
Mobility(DopingDependence HighFieldSaturation NormalElectricField
        CarrierCarrierScattering)
Recombination (SRH (DopingDep ExpTempDep) Auger Avalanche)
EffectiveIntrinsicDensity(Slotboom)
Temperature=298
}

Plot
{
   Doping DonorConcentration AcceptorConcentration eDensity/vector
   hDensity/vector ElectricField/vector eEnormal hEnormal
   eEffectiveField eEffectiveField eEparallel hEparallel
   Current/vector eCurrent/vector hCurrent/vector
   ConductionCurrent/Vector DisplacementCurrent/Vector
   SRHRecombination AugerRecombination TotalRecombination
   AvalancheGeneration eAvalanche hAvalanche Potential
   EquasiFermi hQuasiFermi eGradQuasiFermi hGradQuasiFermi
   IntrinsicDensity EffectiveIntrinsicDensity BandGap
   BandGapNarrowing ConductionBandEnergy ValenceBandEnergy eLifetime
   hLifetime eMobility hMobility SpaceCharge LatticeTemperature
}
Math {
        Extrapolate
        Derivatives
        AvalDerivatives
        Digits=5
        ErReff(electron)=1e10
        ErReff(hole)=1e10
        Iterations=20
}

Solve {
*initial solution
        Poisson
        coupled { poisson electron hole }

*1)ramp from 0V to 550V in steps of 1.21V (2.2e-3)
        QuasiStationary (
                InitialStep=6.55e-3 MaxStep=6.55e-3
                Goal { name="substrate" voltage=550 }
        )
        { coupled { poisson electron hole } }

}
```

```
    wt      = 1.0000e-05   # [cm]
    c2        1.4   # [1]
    alpha   = 90    # [1/cm]
    a0      = -1.0330e-04  # [cm]
    a1        2.7000e-10   # [cm/eV]
    a2      = 4.3300e-17   # [cm/eV^2]
    alpha2    5.5000e-04   # [cm]
    alpha3  = 2.0000e-04   # [cm]
    Ep        3.6   # [eV]
    ,       = 2.0000e-12   # [s]
}
HeavyIon
{ * Generation by a Heavy Ion :
    The temporal distribution is a Gaussian Function
    The radial spatial distrbution can be a exponential, a gaussian
function or give by table
  * The spatial distribution along the path is coming from a table
    G = LET(l)*R(r)*T(t)
    LET(l) = a1 + a2*l + a3 exp(a4*l) + k[c1*(c2 + c3*l)^(c4) +
Lf(l)]
  * with Lf(l) = { Lf1, Lf2, Lf3, ...}
    Lfi are the Lf values for each length lengthi
    if Radial_Exponential_Distribution;
          case 3D   R(r)= exp[-(r/wt)]/ (2*pi*wt^2)
          case 2D   R(r)= exp[-(r/wt)]/ (2*e*wt)
    if Radial_Gaussian_Distribution;
          case 3D   R(r)= exp[-(r/wt)^2]/ (pi*wt^2))
          case 2D   R(r)= exp[-(r/wt)^2]/ (e*wt*Sqrt(pi))
    with wt(l) = { wt1,  wt2,  wt3 ...}
    wti are the wt values for each length lengthi
    e = 1 um
       s_hi    = 2.0000e-12   # [s]
       a_1     - 0.0000e+00   # [carriers/cm^3]
       a_2     = 0.0000e+00   # [carriers/cm^3/cm]
       a_3     = 0.0000e+00   # [carriers/cm^3]
       a_4       0.0000e+00   # [1/um]
       k_hi    = 1     # [1]
       c_1       0.0000e+00   # [carriers/cm^3 or pC/um]
       c_2       0.0000e+00   # [1]
       c_3     = 1     # [1/cm]
       c_4       0.0000e+00   # [1]
    See the manual for more details.
}
VanDortQMModel
{ * dEg = Fit*(13/9)*(epsSi/(4kT))^1/3*(En-EcritQC)^2/3   QM bandgap
shift at inversion surafce,
  * F(d)   2*exp(-(d/dRef)^2)/(1+exp(-2*(d/dRef)^2))   interface
distance function,
  * where En   magnitude of electric field normal to interface,
          d   distance from interface,
          Fit=eFit   vanDort's fitting parameter for electrons,
          Fit=hFit   vanDort's fitting parameter for holes,
          EcritQC=eEcritQC   fitting parameter   critical normal
             electric  field for conduction band correction,
          EcritQC=hEcritQC   fitting parameter   critical normal
             electric field for valence band correction,
          dRef   reference distance from interface.
       eFit    - 2.4000e-08   # [eV*cm]
       hFit      1.8000e-08   # [eV*cm]
       eEcritQC      = 1.0000e+05   # [V/cm]
       hEcritQC        1.0000e+05   # [V/cm]
       dRef      2.5000e-06   # [cm]
    See the manual for more details.
}
Hallscattering
{ ************************** Magnetic Field: ***********************
    mu_n(B)   rn   mu_n;  mu_p(B)   rp * mu_p
  *****************************************************************
       rn      = 1.15  # [1]
       rp        -7.0000e-01  # [1]
}
}
```

2) *Forward Steady-State Characteristic "forward des.cmd"*

```
*********************************************************
# DIODE --> "I-V Static Characteristics Forward"
******************* *************************************
Electrode                          #L=60um
{  { Name="anode" Voltage=0.0 AreaFactor=24.833e3}
   { Name="substrate" Voltage= 0.0 AreaFactor=24.833e3}
}

File
{
       Grid      = "@grid@"           #input
       Doping      "@doping@"         #input
       Current     "@plot@"           #output
       Output   =  "@log@"            #output
       Plot        "@dat@"            #output
       Param       "dessis50ns"
}

Physics
{
Mobility(DopingDependence HighFieldSaturation NormalElectricField
         CarrierCarrierScattering(BrooksHerring))
Recombination (SRH (DopingDep ExpTempDep) Auger Avalanche)
EffectiveIntrinsicDensity(Slotboom)
Temperature=298
}

Plot
{
   Doping DonorConcentration AcceptorConcentration eDensity/vector
```

```
Auger   coefficients:
{ * R_Auger    ( C_n n + C_p p ) ( n p   ni_eff^2)
    with C_n,p    (A + B (T/T0) + C (T/T0)^2) (1 + H exp(-{n,p}/N0))
        A          6.7000e-32   7.2000e-32     # [cm^6/s]
        B          2.4500e-31   4.5000e-33     # [cm^6/s]
        C       = -2.2000e-32 ,         2.6300e-32     # [cm^6/s]
        H       = 3.46667 ,      8.25688 # [1]
        N0         1.0000e+18   1.0000e+18     # [cm^(-3)]
}
TrapAssistedAuger   lifetimes:
{ * 1/tau_TAA = : ( n + p )
                1.0000e-12   1.0000e-12     # [cm^3/s]
}
TrapAssistedTunneling   lifetimes:
{ * See Dessis manual `Trap-Assisted Tunneling'
        S          3.5    # [1]
        hbarOmega      = 0.068 # [eV]
        TrapFraction   = 0.01  # [1]
        Z          0.0000e+00    # [1]
        MinField          1.0000e+03    # [V/cm]
}
CDL   Recombination:
{ * See Simul manual 'Coupled  Defect-Level Recombination
    Here: Variable   value for trap1 , value for trap2  # [units]
        Etrap     0.0000e+00 , 0.0000e+00     # [eV]
        e_taumin        = 0.0000e+00   0.0000e+00     # [s]
        e_taumax        = 1.0000e-05 , 1.0000e-05     # [s]
        e_Nref  = 1.0000e+16   1.0000e+16     # [cm^(-3)]
        e_gamma = 1     1        # [1]
        e_Talpha          -1.5000e+00 ,        -1.5000e+00     # [1]
        e_Tcoeff          2.55 ,         2.55     # [1]
        h_taumin          0.0000e+00   0.0000e+00     # [s]
        h_taumax          3.0000e-06 , 3.0000e-06     # [s]
        h_Nref   1.0000e+16   1.0000e+16     # [cm^(-3)]
        h_gamma = 1     1        # [1]
        h_Talpha          -1.5000e+00 ,        -1.5000e+00     # [1]
        h_Tcoeff          2.55 ,         2.55     # [1]
        TrapTrapRate      1.0000e+15    # [cm^-3 s^-1]
        S         2     2        # [1]
        hbarOmega         0.068          0.068     # [eV]
        MinField          10     # [V/cm]
}
vanOverstraetendeMan   Impact Ionization:
{ * G_impact   alpha_n n v_drift_n     alpha_p p v_drift_p
    with alpha   gamma a  exp(-b gamma/E) for E<E0 (low) and E>E0
(high)
  *  with gamma   tanh(hbarOmega/(2kT0)) / tanh(hbarOmega/(2kT))
        a(low)    7.0300e+05   1.5820e+06     # [1/cm]
        a(high) = 7.0300e+05   6.7100e+05     # [1/cm]
        b(low)    1.2310e+06   2.0360e+06     # [V/cm]
        b(high) = 1.2310e+06   1.6930e+06     # [V/cm]
        E0      = 4.0000e+05 , 4.0000e+05     # [V/cm]
        hbarOmega         0.063 # [eV]
}
OkutoCrowell   Impact Ionization:
{ * G_impact = alpha_n n v_drift_n  +  alpha_p p v_drift_p
    with alpha   a (1+c(T-300)) E exp[-(b (1+d(T-300)) /E )^2]
        a         0.426 ,      0.243   # [1/cm]
        b         4.8100e+05   6.5300e+05     # [V/cm]
        c         3.0500e-04   5.3500e-04     # [1/K]
        d         6.8600e-04   5.6700e-04     # [1/K]
}
Lackner   Impact Ionization:
{ * G_impact   alpha_n n v_drift_n  +  alpha_p p v_drift_p
    with alpha = a_x gamma / Z exp(-b_x gamma / E)   ,  x=n,p
    with gamma = tanh(hbarOmega/(2kT0)) / tanh(hbarOmega/(2kT))
    and Z = 1 + b_n gamma / E exp(-b_n gamma / E)   b_p gamma / E
exp(-b_p gamma / E)
        a        = 1.3160e+06   1.8180e+06     # [1/cm]
        b        = 1.4740e+06 , 2.0360e+06     # [V/cm]
        hbarOmega        0.063 # [eV]
}
Antoniadis   Impact Ionization:
{ * See Dessis manual `Antoniadis Avalanche Generation'
        Eth        2 ,   3.5       # [eV]
        C_sub      2.0000e+14   4.0000e+12     # [1/s]
        Chi_n_1 = 3.0000e+05    # [K^1/5 eV^-3]
        Chi_n_2 = 5.0000e+04    # [K^1/5 eV^-3]
        Chi_p   = 4.6000e+04    # [K^1/5 eV^-3]
        C_weight         2.5000e-10    # [1]
}
Band2BandTunneling
{ * See Dessis manual `Band-To-Band Tunneling'
        A          8.9770e+20    # [cm / (s V^2)]
        B          2.1466e+07    # [eV^(-3/2) V/cm]
        hbarOmega       = 0.0186       # [eV]
   Traditional models for the following keywords in input file:
Band2Band(E1)    A1*E*exp(-B1/E)
 * Band2Band(E1_5): A1_5*E^1.5*exp(-B1_5/E)
   Band2Band(E2)   : A2*E^2*exp(-B2/E)
        A1      = 1.1000e+27    # [1/cm/sec/V]
        B1      = 2.1300e+07    # [V/cm]
        A1_5    = 1.9000e+24    # [1/cm/sec/V^1.5]
        B1_5    = 2.1900e+07    # [V/cm]
        A2      = 3.5000e+21    # [1/cm/sec/V^2]
        B2        2.2500e+07    # [V/cm]
}
AlphaParticle
{ * Generation by an alpha particle with energy E:
    G   1/Sqrt(2 pi s^2) exp( -1/2 ((t-tm)/s)^2) *
          scale exp[-1/2 ( (v^2+w^2)/wt^2 )] *
           { c1 exp[alpha u] + c2 exp[ -1/2 ( (u-alpha1)/alpha2 )^2 ]}
    if u<alpha1+alpha3; G=0 else.
    with alpha1   a0 + a1 E + a2 E^2, c1   exp[alpha*(alpha1[10MeV]-
alpha1[E]]
  * scale from generated e-h pairs    E/Ep
```

```
{   Philips Unified Mobility Model:
        mumax_As        = 1.4170e+03    # [cm^2/Vs]
        mumin_As        = 52.2  # [cm^2/Vs]
        theta_As        = 2.285 # [1]
        n_ref_As        = 9.6800e+16    # [cm^-3]
        alpha_As        = 0.68  # [1]
        mumax_P         = 1.4140e+03    # [cm^2/Vs]
        mumin_P         = 68.5  # [cm^2/Vs]
        theta_P         = 2.285 # [1]
        n_ref_P         = 9.2000e+16    # [cm^-3]
        alpha_P         = 0.711 # [1]
        mumax_B         = 4.7050e+02    # [cm^2/Vs]
        mumin_B         = 44.9  # [cm^2/Vs]
        theta_B         = 2.247 # [1]
        n_ref_B           2.2300e+17    # [cm^-3]
        alpha_B           0.719 # [1]
        nref_D            4.0000e+20    # [cm^(-3)]
        nref_A            7.2000e+20    # [cm^(-3)]
        cref_D            0.21  # [1]
        cref_A          - 0.5   # [1]
        me_over_m0        1     # [1]
        mh_over_m0        1.258 # [1]
        f_CW              2.459 # [1]
        f_BH              3.828 # [1]
}
EnormalDependence:
{ * mu_Enorm^(-1) = mu_ac^(-1) + mu_sr^(-1)  with:
    mu_ac = B / Enorm + C (T/T0)^(-1) (N/N0)^lambda / Enorm^(1/3) )
    mu_sr^-1 = Enorm^(A+alpha*n/N^nu) / delta + Enorm^3 / eta
    EnormalDependence is added with factor exp(-l/l_crit), where l is
    the distance to the nearest point of DES_c_Si/DES_c_SiO2
interface. Factor is
  * equal to 1 if l_crit > 100.
        B          4.7500e+07   9.9250e+06      # [cm/s]
        C          5.8000e+02   2.9470e+03      # [cm^5/3/(sV^2/3)]
        N0       - 1 ,   1          # [cm^-3]
        lambda     0.125        0.0317  # [1]
        delta      5.8200e+14   2.0546e+14      # [V/s]
        A          2 ,   2          # [1]
        alpha    = 0.0000e+00   0.0000e+00      # [1]
        nu       = 1 ,   1          # [1]
        eta      = 5.8200e+30   2.0546e+30      # [V^2/cm*s]
        l_crit   = 1.0000e-06   1.0000e-06      # [cm]
}
CarrierCarrierScattering
{ * with Conwell/Weisskopf screening:
    mu_cc = D (T/T0)^3/2 / sqrt(n p) [ln( 1   F (T/T0)^2 (n p)^(-
1/3)]^(-1)
        D          1.0400e+21   # [(cmVs)^(-1)]
        F          7.4520e+13   # [1]
    with Brooks/Herring screening:
    mu_cc    c1 (T/T0)^1.5 / ( Sqrt(n,p) ( ln(1+eta)   eta / (1+eta) )
}
```

```
        with   eta   c2(T/T0)^2/(n+p)
          c1      = 1.5600e+21   # [(cmVs)^(-1)]
          c2        7.6300e+19   # [cm^(-3)]
}
HighFieldDependence:
{ * Caughey-Thomas model:
    mu_highfield = mu_lowfield / ( 1 + (mu_lowfield E / vsat)^beta
)^1/beta
  * beta   beta0 (T/T0)^betaexp.
        beta0   = 1.109         1.213   # [1]
        betaexp = 0.66          0.17    # [1]
    Transferred-Electron Effect:
    mu_highfield
(mu_lowfield+(vsat/E)*(E/E0_TrEf)^4)/(1+(E/E0_TrEf)^4)
        E0_TrEf = 4.0000e+03   4.0000e+03     # [1]
        Ksmooth_TrEf   = 1 ,   1        # [1]
   For vsat either Formula1 or Formula2 can be used.
        Vsat_Formula     1     1        # [1]
   Formula1 for saturation velocity:
            vsat = vsat0 (T/T0)^(-Vsatexp)
   (Parameter Vsat_Formula has to be not equal to 2):
        vsat0     1.0700e+07   8.3700e+06     # [1]
        vsatexp = 0.87 ,       0.52     # [1]
   Formula2 for saturation velocity:
            vsat   A_vsat   B_vsat*(T/T0)
   (Parameter Vsat_Formula has to be equal to 2):
        A_vsat  = 1.1300e+07   1.1300e+07     # [1]
        B_vsat    3.6000e+06 , 3.6000e+06     # [1]
        vsat_min       = 5.0000e+05   5.0000e+05     # [1]
}
HydroHighFieldDependence:
{ * mu_hf   mu / ( 1   (3*mu/(2*vsat^2*tau_e)   (Tc-Tl))^beta
)^1/beta
  * Tc=carrier temperature; Tl=lattice temperature
    beta   beta0 (Tl/T0)^betaexp; vsat   vsat0 (Tl/T0)^(-Vsatexp);
    Only for the Meinerzhagen-Engl model (ED-35, pp. 689-697)
        beta0   = 0.6   0.6      # [1]
        betaexp = 0.01 ,        0.01    # [1]
        vsat0   = 1.0700e+07    8.3700e+06     # [1]
        vsatexp = 0.87          0.52    # [1]
}
Scharfetter   relation and trap level for SRH recombination:
{ * tau   taumin + ( taumax   taumin ) / ( 1   ( N/Nref )^gamma
    tau(T)   tau * ( (T/300)^Talpha )           (TempDep)
    tau(T)   tau   exp( Tcoeff * ((T/300)-1) ) (ExpTempDep)
        taumin    0.0000e+00   0.0000e+00     # [s]
        taumax    5.0000e-06   5.0000e-06     # [s]
        Nref      7.0000e+16   7.0000e+16     # [cm^(-3)]
        gamma     1     1        # [1]
        Talpha    -1.5000e+00         -1.5000e+00    # [1]
        Tcoeff  = 2.55 ,       2.55     # [1]
        Etrap   = 0.0000e+00   # [eV]
}
```

```
    hEeff   hEeff / p_l_f  ( or b   b*p_l_f )
    Additional coefficients n_gamma, p_gamma, n_delta, p_delta
      n_l_f   = 1     # [1]
      p_l_f     1     # [1]
      n_gamma = 1     # [1]
      p_gamma = 1     # [1]
      n_delta = 1.5   # [1]
      p_delta = 1.5   # [1]
}
TEPower
{
      s_n       1     # [1]
      s_p     = 1     # [1]
      scale_n = 1     # [1]
      scale_p = 1     # [1]
}
Ionization
{
      E_As_0    0.054 # [eV]
      alpha_As      = 3.1000e-08   # [eV cm]
      g_As    - 2     # [1]
      E_P_0   = 0.045 # [eV]
      alpha_P = 3.1000e-08   # [eV cm]
      g_P     = 2     # [1]
      E_Sb_0  = 0.039 # [eV]
      alpha_Sb      = 3.1000e-08   # [eV cm]
      g_Sb      2     # [1]
      E_B_0     0.045 # [eV]
      alpha_B       = 3.1000e-08   # [eV cm]
      g_B       4     # [1]
      E_In_0    0.16  # [eV]
      alpha_In      = 3.1000e-08   # [eV cm]
      g_In      4     # [1]
}
      Bandgap *temperature dependent*
      { * Eg = Eg0   alpha T^2 / (beta + T)
          Eg0 can be overwritten in below Band Gap Narrowing
          models, if any of the BGN model is chosen in physics
section
              Eg0      1.16964     # [eV]
              Chi0     4.05 # [eV]
              alpha    4.7300e-04  # [eV K^-1]
              beta     6.3600e+02  # [K]
      }
OldSlotboom
{ * deltaEg = Ebgn ( ln(N/Nref) + [ (ln(N/Nref))^2 + 0.5]^1/2 )
      Eg0      1.15369     # [eV]
      Ebgn     9.0000e-03  # [eV]
      Nref   = 1.0000e+17  # [cm^-3]
}
Slotboom
{ * deltaEg   Ebgn ( ln(N/Nref) + [ (ln(N/Nref))^2 + 0.5]^1/2 )
      Eg0      1.164845    # [eV]
```

```
        Ebgn     6.9200e-03   # [eV]
        Nref     1.3000e+17   # [cm^-3]
}
delAlamo
{   deltaEg = Ebgn  ln(N/Nref)
        Eg0    = 1.15557      # [eV]
        Ebgn   = 0.0187       # [eV]
        Nref   = 7.0000e+17   # [cm^-3]
}
Bennett
{ * deltaEg   Ebgn (ln(N/Nref))^2
        Eg0      1.16964      # [eV]
        Ebgn     6.8400e-03   # [eV]
        Nref     3.1620e+18   # [cm^-3]
}
        eDOSMass
        { * me = [ (6   mt)^2    ml ]^(1/3)
                mt = a Eg(0)/Eg(T)  m0
              a       = 0.1905       # [1]
              ml      = 0.9163       # [1]
        }
        hDOSMass
        { * mh   [(a+bT+cT^2+dT^3+eT^4)/(1+fT+gT^2+hT^3+iT^4)]^(2/3)
m0
              a         0.443587     # [1]
              b       = 0.003609528  # [K^-1]
              c       = 0.0001173515 # [K^-2]
              d       = 1.263218e-06 # [K^-3]
              e       = 3.025581e-09 # [K^-4]
              f         0.004683382  # [K^-1]
              g         0.0002286895 # [K^-2]
              h         7.469271e-07 # [K^-3]
              i         1.727481e-09 # [K^-4]
        }
ConstantMobility:
{ * mu_const   mumax (T/T0)^(-Exponent)
        mumax   = 1.4170e+03   4.7050e+02    # [cm^2/(Vs)]
        Exponent      = 2.5    2.2     # [1]
}
DopingDependence:
{ * mu_dop = mumin1 exp(-Pc/N) + (mu_const   mumin2)/(1+(N/Cr)^alpha)
                                   mu1/(1+(Cs/N)^beta)
    with mu_const from ConstantMobility
        mumin1    52.2         44.9     # [cm^2/Vs]
        mumin2    52.2         0.0000e+00    # [cm^2/Vs]
        mu1     = 43.4 ,       29       # [cm^2/Vs]
        Pc      = 0.0000e+00   9.2300e+16    # [cm^3]
        Cr      = 9.6800e+16   2.2300e+17    # [cm^3]
        Cs      = 3.4300e+20   6.1000e+20    # [cm^3]
        alpha   = 0.68 ,       0.719    # [1]
        beta    = 2     2          # [1]
}
PhuMob:
```

```
  MinElementWidth = 3
  MinElementHeight   0.2
  MaxTransDiff = (DopingConcentration, 0.5 )
 }
 {
  top = -44
  left = -1
  bottom = 0
  right   61
  MaxElementWidth   15
  MaxElementHeight = 2.5
  MinElementWidth   10
  MinElementHeight = 1
  MaxTransDiff = (DopingConcentration, 0.5 )
 }
 {
  top   -44
  left   -3
  bottom   -43.3
  right = 63
  MaxElementWidth = 10
  MaxElementHeight = 0.4
  MinElementWidth = 5
  MinElementHeight   0.2
  MaxTransDiff = (DopingConcentration, 0.5 )
 }
}
  SubMesh
  {
   Geofile = "n1_dio.grd.gz"
   Datafile   "n1_dio.dat.gz"


   win_top =-43.84
   win_left =0
   win_bottom =625
   win_right =60
  }
Profiles
{
}
```

B.3. Input Command Flies of the Device and System Simulation

1) *Device template parameter file "dessis.par"*

```
Material   "Silicon" {
Epsilon
{ *  Ratio of the permittivities of material and vacuum
     epsilon = 11.7 # [1]
}
LatticeHeatCapacity
{ *  lumped electron-hole-lattice heat capacity
     cv     = 1.63 # [J/(K cm^3)]
}
Kappa
{ *  Lattice thermal conductivity

  kappa = 1 / ( Si_a + Si_b   T + Si_c   T^2 )
     Si_a   = 0.03 # [K cm/W]
     Si_b     1.5600e-03   # [cm/W]
     Si_c     1.6500e-06   # [cm/(W K)]
}
CarrierThermalConductivity
{ *  Lower limit for the carrier thermal conductivities,
     expressed as a fraction of the lattice
     thermal conductivity K_L (i.e. of kappa, see above)
       K_n/K_L = 1.0000e-34   # [1]
       K_p/K_L = 1.0000e-34   # [1]
}
EnergyRelaxationTime
{    Energy relaxation times in picoseconds
       (tau_w)_ele      0.45  # [ps]
       (tau_w)_hol      0.3   # [ps]
}
EnergyFlux
{ *  Coefficient in front of the energy flux equation
     energy_flux_coef=0.6 corresponds to Stratton model
       energy_flux_coef_ele    0.6   # [1]
       energy_flux_coef_hol    0.6   # [1]
}
ThermalDiffusion
{ *  Thermal diffusion factor (0 <= td <= 1)
     td=0. corresponds to Stratton model
       td_n     0.0000e+00    # [1]
       td_p     0.0000e+00    # [1]
}
HeatFlux
{ *  Heat flux factor (0 <= hf <= 1)
       hf_n     1     # [1]
       hf_p     1     # [1]
}
AvalancheFactors
{ *  Coefficientss for avalanche generation with hydro
     Factors n_l_f, p_l_f for energy relaxation length in the
expressions
   *  for effective electric field for avalanche generation
     eEeff   eEeff / n_l_f   ( or b = b*n_l_f )
```

```
    bottom = -43.5
    right   63
    MaxElementWidth = 10
    MaxElementHeight   0.4
    MinElementWidth = 5
    MinElementHeight   0.2
    MaxTransDiff   (DopingConcentration, 0.5 )
   }
   {
    top   -16
    left   -3
    bottom   -6
    right = 63
    MaxElementWidth   10
    MaxElementHeight   0.8
    MinElementWidth   3
    MinElementHeight   0.4
    MaxTransDiff = (DopingConcentration, 0.5 )
   }
   {
    top   -42
    left   -3
    bottom   -40
    right = 63
    MaxElementWidth   10
    MaxElementHeight   0.5
    MinElementWidth = 3
    MinElementHeight   0.2
    MaxTransDiff = (DopingConcentration, 0.5 )
   }
}
    SubMesh
    {
      Geofile   "n1_dio.grd.gz"
      Datafile   "n1_dio.dat.gz"
      win_top =-43.84
      win_left =0
      win_bottom =625
      win_right =60
    }
Profiles
{
}
```

(b) Modified Mosaic Contact P-i-N Diode Structure

"*_mdr.cmd"

```
Title "M-MCPD: n1"
Refinement
{
   MaxElementWidth = 20
   MaxElementHeight   100
   MinElementWidth   15
   MinElementHeight = 50
   MaxTransDiff   (DopingConcentration, 0.5 )
  {
   top = -42
   left - -3
   bottom = -41.5
   right   13
   MaxElementWidth   10
   MaxElementHeight   0.5
   MinElementWidth   3
   MinElementHeight   0.2
   MaxTransDiff = (DopingConcentration, 0.5 )
  }
  {
   top   -45
   left = 12.5
   bottom   -38.5
   right   17
   MaxElementSize   0.5
   MinElementSize   0.2
   MaxTransDiff = (DopingConcentration, 0.5 )
  }
  {
   top   -15.5
   left   -3
   bottom   -8
   right = 63
   MaxElementWidth   10
   MaxElementHeight = 0.8
   MinElementWidth   3
   MinElementHeight = 0.4
   MaxTransDiff   (DopingConcentration, 0.5 )
  }
  {
   top = -40
   left   13
   bottom = -38.5
   right   63
   MaxElementWidth   10
   MaxElementHeight   0.5
   MinElementWidth = 3
   MinElementHeight   0.2
   MaxTransDiff = (DopingConcentration, 0.5 )
  }
  {
   top   -31.5
   left = -3
   bottom   -29
   right = 63
   MaxElementWidth = 10
   MaxElementHeight   0.5
```

```
                !******  PREDEPOSITION  ******
Diffusion(TIME=20min, TEMPERATURE=1100degC, ELEMENT=B
CONCENTRATION=5.5e+18)
1d(xsec(0), RS=on)
             !******  DRIVE-IN DIFFUSION BORON P-  ******
Diffusion(TIME=5.66min, TEMPERATURE= 750degC, FLOW(O2=.3201/min,
N2=41/min))
Diffusion(TempRATE=282.5K/min, TEMPERATURE=(750,1200),
FLOW(O2=.3201/min, N2=41/min))
Diffusion(TIME=1050min, TEMPERATURE=1200degC, FLOW(O2=.3201/min,
N2=41/min))
1d(xsec(0), RS=on)
Diffusion(TempRate=277.65K/min, TEMPERATURE=(1200degC,900degC),
FLOW(O2=5.261/min, N2=41/min))
Diffusion(TIME=4min, TEMPERATURE=900degC, atmo=O2,
FLOW(O2=5.261/min))
Diffusion(TIME=1.5min, TEMPERATURE=900degC, atmo=H2,
FLOW(O2=5.261/min, H2=101/min))
Diffusion(TIME=60min, TEMPERATURE=(900), atmo=H2O, FLOW(O2=5.261/min,
H2=101/min))
Diffusion(TIME=1.75min, TEMPERATURE=(900))
Diffusion(TempRate=276.65K/min, TEMPERATURE=(900,750),
FLOW(N2=91/min))
1d(xsec(0), RS=on)
             !******  MASKING P+ REGIONS PROCESS  ******
MASK(MATERIAL=la, THICKNESS=1.5um, X(-5, 15))
ETCH(MATERIAL=OX, STOP=sigas, rate(MATERIAL=OX,a0=500), OVER=50)
ETCH(MATERIAL=la)
         !******  PREDEPOSITION OF PHOSPHORUS ANODE  ******
DIFFusion(TIME=12, TEMPERATURE=1200, Element=P,Concentration=1.5e20)
1d(xsec(0), RS=on)
etch(material=ox, STOP=sigas)
             !******  MASKING N+ REGIONS PROCESS  ******
DEPOSIT(MATERIAL=OX, THICKNESS=0.5um)
MASK(MATERIAL=la, THICKNESS=1.5um, X(15, 65))
ETCH(MATERIAL=OX, STOP=sigas, rate(MATERIAL=OX,a0=500), OVER=50)
ETCH(MATERIAL=la)
!******  PREDEPOSITION OF BORON ANODE  ******
DIFFusion(TIME=50, TEMPERATURE=1200, Element=B, Concentration=1.8e19)
1d(xsec(0), RS=on)
                   !******  Removing SIO2  ******
etch(material=ox, STOP=sigas)
                       !******  Save  ******
      save(file=n@node@,type=mdraw,
      MaxElementWidth=10,
      MaxElementHeight=40,
      MinElementWidth=5,
      MinElementHeight=10,
          contacts(
                contact1(name=anode, Location=TopRight)
                contact2(name=substrate, Location=Bottom)
                )
          )
      save(file='n@node@',type=Picasso)
      1d(file=n@node@-ppnn, spe(net), xsec(8.0), fact=-1, noappend)
      1d(file=n@node@-npnn, spe(net), xsec(37.0), fact=-1, noappend)
quit
```

B.2. Input Command Flies of the Structure and Mesh Generator

a) *Modified P-i-N Diode Structure*

*"*_mdr.cmd"*

```
Title "M-PiN Conventional: n1"
Refinement
{
   MaxElementWidth   20
   MaxElementHeight = 100
   MinElementWidth = 15
   MinElementHeight   50
   MaxTransDiff    (DopingConcentration, 0.5 )
  {
   top = -44
   left   -1
   bottom = 0
   right   61
   MaxElementWidth = 15
   MaxElementHeight   2.5
   MinElementWidth = 10
   MinElementHeight   1
   MaxTransDiff    (DopingConcentration, 0.5 )
  }
  {
   top   -31
   left   -3
   bottom   -29.5
   right   63
   MaxElementWidth = 10
   MaxElementHeight   0.5
   MinElementWidth = 3
   MinElementHeight = 0.2
   MaxTransDiff = (DopingConcentration, 0.5 )
  }
  {
   top   -44
   left   -3
```

Appendix B

B.1. Input Command Flies "dio.cmd" of the Process Technological Simulation

a) *Modified P-i-N Diode Structure*

```
Title('M-PiN: n@node@', mpoints =14000, maxv=50000, maxlst=1000,
newdiff=1, SiDiff=on)
repl(cont(maxtrl=7, markm=-10, markmax=-0, markj=-7, markg=-8))
repl(Contr(ngra=10, nprint=1, lprot=1))
                !****** STATRTING SUBSTRATE ******
grid(xleft=0, xright=60, ybottom=-345, ytop=100, nx=20)
substrate(elem=P, orien=111, concentration=2.2e19)

diff:(moddiff=conventional, Si(B(moddiff=SUPREM-3)),
Si(P(moddiff=SUPREM-3)))
                 !****** PREABAKE PROCESS ******
DIFFusion(ATMO=PREB, Time=15, TEMPERATURE=1100,    GAS=(P(PHS=1e-
10)), TTRAN=0.5)
                  !****** EPITAXIAL LAYER ******
DIFFusion(ATMO=EPI, GrowthRate=2000, Time=22min, ELEMENT=P,
CONCENTRATION=2.0e14, PP=2.74, dthickness=0.1um, TEMPERATURE=1100,
SiGas(P(BCtyp=Segregation, ka0=2.e-5, kaw=0)))
                   !****** PREDEPOSITION ******
Diffusion(TIME=20min, TEMPERATURE=1100degC, ELEMENT=B
CONCENTRATION=5.5e+18)
1d(xsec(0), RS=on)
             !****** DRIVE-IN DIFFUSION BORON P- ******
Diffusion(TIME=5.66min, TEMPERATURE= 750degC, FLOW(O2=.3201/min,
N2=41/min))
Diffusion(TempRATE=282.5K/min, TEMPERATURE=(750,1200),
FLOW(O2=.3201/min, N2=41/min))
Diffusion(TIME=1050min, TEMPERATURE=1200degC, FLOW(O2=.3201/min,
N2=41/min))
1d(xsec(0), RS=on)
Diffusion(TempRate=277.65K/min,TEMPERATURE=(1200degC,900degC),
FLOW(O2=5.261/min, N2=41/min))
Diffusion(TIME=4min, TEMPERATURE=900degC, atmo=O2,
FLOW(O2=5.261/min))
Diffusion(TIME=1.5min, TEMPERATURE=900degC, atmo=H2,
FLOW(O2=5.261/min, H2=101/min))
Diffusion(TIME=60min,        TEMPERATURE=(900),  atmo=H2O,
FLOW(O2=5.261/min, H2=101/min))
Diffusion(TIME=1.75min, TEMPERATURE=(900))
Diffusion(TempRate=276.65K/min, TEMPERATURE=(900,750),
FLOW(N2=91/min))
1d(xsec(0), RS=on)
                   !****** Removing SIO2 ******
etch(material=ox)
           !****** PREDEPOSITION OF BORON ANODE ******
DIFFusion(TIME=50min, TEMPERATURE=1200degC, Element=B,
Concentration=1.8e+19)
1d(xsec(0), RS=on)
                      !****** Save ******
        save(file=n@node@,type=mdraw,
        MaxElementHeight=40,
        MinElementHeight=10,
        MaxElementWidth=10,
        MinElementWidth=5,
             contacts(
                   contact1(name=anode, Location=TopRight)
                   contact2(name=substrate, Location=Bottom)
                   )
             )
        save(file='n@node@',type=Picasso)
        1d(file=n@node@, spe(net), xsec(30.0), fact=-1, noappend)
quit
```

(b) *Modified Mosaic Contact P-i-N Diode Structure*

```
Title('M-MCPD: n@node@', mpoints =14000, maxv=50000, maxlst=1000,
newdiff=1, SiDiff=on)
repl(cont(maxtrl=7, markm=-10, markmax=-0, markj=-7, markg=-8))
repl(Contr(ngra=10, nprint=1, lprot=1))
                !****** STATRTING SUBSTRATE ******
grid(xleft=0, xright=60, ybottom=-345, ytop=100, nx=20)
substrate(elem=P, orien=111, concentration=2.2e19)

diff:(moddiff=conventional, Si(B(moddiff=SUPREM-3)),
Si(P(moddiff=SUPREM-3)))
                 !****** PREABAKE PROCESS ******
DIFFusion(ATMO=PREB, Time=15, TEMPERATURE=1100, GAS=(P(PHS=1e-10)),
TTRAN=0.5)
                 !****** PREABAKE PROCESS ******
DIFFusion(ATMO=EPI, GrowthRate=2000, Time=22min, ELEMENT=P,
CONCENTRATION=2.0e14, PP=2.74, dthickness=0.1um, TEMPERATURE=1100,
SiGas(P(BCtyp=Segregation, ka0=2.e-5, kaw=0)))
```

layer, sg_2 the segregation coefficient and h_2 the flux parameter between c_{tot} and m. A flux parameter condition is assumed also between adsorption layer and gas:

$$j_{Gas} = h_1(sg_1 P - m) \tag{A.9}$$

P denotes the partial pressure in the gas at the interface to the adsorption layer, sg_1 and h_1 the segregation constant and the flux parameter between P and m. Neglecting the diffusion inside the adsorption layer, one obtains the following balance equation in the adsorption layer:

$$\frac{dm}{dt} = j_{Si} + j_{Gas} \tag{A.10}$$

where the initial concentrations are defined externally or from a previous prebake simulation. If one assumes that the dopant flux from the gas into the adsorption layer is compensated from the main gas flow, one has:

$$j_{Gas} \approx k_m(P^\infty - P) \tag{A.11}$$

where P^∞ denotes the partial pressure in the main gas flow and k_m the flux parameter. The partial pressure at the adsorption layer is defined from (A.9) and (A.11) as:

$$P = \frac{k_m}{h_1 sg_1 + k_m} P^\infty + \frac{h_1}{h_1 sg_1 + k_m} m \quad \textit{and so for } j_{Gas} \textit{ yield}$$

$$j_{Gas} = \frac{h_1 k_m}{h_1 sg_1 + k_m}\left(sg_1 P^\infty - m\right) \tag{A.12}$$

In addition, it is assumed, that except at the starting time, the concentrations at the adsorption layer and the substrate are in equilibrium e.g.

$$m = sg_2 c_{tot} \tag{A.13}$$

From (A.10) together with (A.8), (A.12) and (A.13) one obtains the boundary condition for (A.7) at the interface to the gas

$$D\frac{\partial c_{tot}}{\partial n} = -\frac{k_m h_1 sg_1}{h_1 sg_1 + k_m} P^\infty + \left(\frac{h_1 k_m sg_2}{h_1 sg_1 + k_m} + g\right) c_{tot} + sg_2 \frac{dc_{tot}}{dt} \tag{A.14}$$

and, merging the parameters:

$$D\frac{\partial c_{tot}}{\partial n} = -h_3\left(P^\infty - \frac{c_{tot}}{sg_3}\right) + g c_{tot} + sg_2 \frac{dc_{tot}}{dt} \tag{A.15}$$

$$D = D^{+}\frac{n_{ie}}{n} + D^{X} + D^{-}\frac{n}{n_{ie}} + D^{=}\left(\frac{n}{n_{ie}}\right) + D_{I}[I] \tag{A.5}$$

If one assumes, that the ionization reactions of the point defects are in equilibrium, the densities of the charged point defects can be expressed by the concentration of the neutral defects, the electron density n and the effective intrinsic density n_{ie}.

In the conventional models of DIOS-ISE the only dependency on the silicon interstitial concentration is assumed for diffusion in oxidizing atmosphere (by default only for boron and antimony). The oxidation enhanced diffusion of boron is computed as:

$$D_{I}[I](x,y) = D0\left|\mathbf{v}_{\Gamma}(x_{\Gamma} y_{\Gamma})\right|^{voxn} \exp - \frac{\sqrt{(x-x_{\Gamma})^{2} + (y-y_{\Gamma})^{2}}}{leny} \tag{A.6}$$

where (x,y) denotes a point in the silicon region, (x_{Γ},y_{Γ}) the closest point on an oxidation front in interface, v_{Γ} the velocity of that interface and **D0**, *voxn* and *leny* experimental parameters.

A.2. Epitaxy [75]

For *Atmosphere=Epitaxy* the growth of monocrystalline silicon layers, together with the dopant deposition and redistribution is simulated. A chemical vapor deposition technique (CVD) has been used as reference to develop the epitaxy model. The deposition rate of silicon is prescribed externally and the dopant distribution has to be simulated in the substrate region, assuming an initial distribution from previous process steps and in the newly deposited layer. The deposition is assumed along the entire surface of the substrate region. A homogeneous doping in the epitaxy layer usually cannot be achieved in the vicinity of the initial substrate surface. The transition region is defined by the dopant concentrations in the adsorption layer, which can be used to explain the auto-doping effect, and by the dopant diffusion in the growing substrate. After a transient period for a given partial pressure, a constant doping level is achieved. An inhomogeneous doping level can be achieved using a time dependent partial pressure. Due to the rapid growth of the layer the dopant loss from highly doped regions into the gas phase is of minor importance, in particular there are no extremely high concentrations obtained at the initial substrate surface. Thus the lateral transport in the gas phase is neglected in DIOS-ISE. The dopant redistribution in the substrate and the already grown epilayer is described by

$$\frac{\partial c_{tot}}{\partial t} = -\operatorname{div}\mathbf{j} \tag{A.7}$$

together with the initial condition $c_{tot}(x,y,0)=c_{tot}^{0}(x,y)$, the flux parameter condition

$$j_{Si} = -D\frac{\partial c_{act}}{\partial n} - g c_{act} = h_{2}(sgc_{act} - m) \tag{A.8}$$

at the moving adsorption layer and Neumann or Dirichlet conditions everywhere else. c_{tot} denotes the total dopant concentration, D the diffusivity, depending on all dopant concentrations and the temperature, g the growth rate, e.g. the velocity of the phase boundary in the direction of the outer normal, which is usually assumed to be constant. m denotes the dopant concentration in the adsorption

Appendix A

Conventional Diffusion Model In Silicon and Epitaxial Growth

A.1. Conventional Diffusion Models In Silicon [75]

In silicon, for each of the dopants the total c_{tot} and the active c_{act} concentrations are distinguished. Active dopants are assumed to be electrically singly charged and to be the only mobile dopant species. The diffusion equation reads

$$\frac{\partial c_{tot}}{\partial t} + \operatorname{div} \mathbf{j} = 0 \tag{A.1}$$

where the dopant flux **j** is defined as

$$j = -D(\operatorname{grad} c_{act} + q c_{act} \operatorname{grad} \varphi) \tag{A.2}$$

Here D denotes the diffusion coefficient, q the charge state (q=+1 for donors; q=-1 for acceptors) and φ the suitably scaled electrostatic potential. The intrinsic carrier density in silicon is assumed to be given by:

$$n_i = T^{3/2} NI0 \exp\left(-\frac{NIE}{kT}\right) \tag{A.3}$$

Where **NI0** is the preexponential factor for the intrinsic carrier density, and **NIE** is the activation energy for the intrinsic carrier density. In order to account the impact of high dopant concentrations on the band gap in silicon, a reduction of the band gap can be specified depending on the local total concentration for each of the dopants. As a result an effective intrinsic density of electrons and holes is computed:

$$n_{ie} = ni \prod_{dopants} \exp\left(-\frac{\Delta E_g c_{tot}}{2kTc^*_{Si}}\right) \tag{A.4}$$

Here c^*_{Si} is the concentration of host lattice atoms ($5\text{x}10^{22}\text{cm}^{-3}$). Due to missing data, all default values of ΔEg (in the input syntax **DEG**) still remain zero. Interactions of dopant atoms and point defects (silicon interstitials I and vacancies V) are assumed to be the driving force for the dopant diffusion. In the conventional models DIOS$_{\text{-ISE}}$ neglects the kinetics of the point defects and describes the dopant flux by a phenomenological law (A.2). All interaction with point defects (vacancies) is expressed only in the assumptions for the diffusivities. The vacancies are assumed to exist in various charge states (V^X – neutral, $V^{\pm}$ – singly negatively or positively charged and $V^{=}$ – doubly negatively charged). The dopant diffusivities are assumed to be given as:

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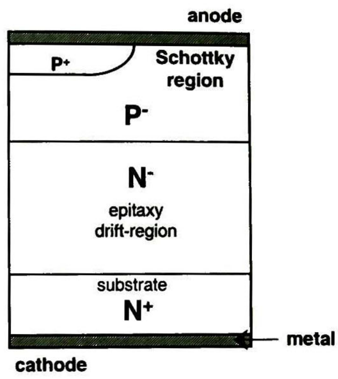


Figure 5.1: *Modified Mosaic Contact PiN/Schottky Diode (M-MCPSD).*

Form the comparative results of the simulated reverse *I-V* characteristics it can be seen that, both the modified MCPD rectifier and the M-PiN rectifier can withstand reverse bias voltage of more than 350V at 300K. Therefore, the minimum blocking voltage of 200V is guaranteed.

Although it was expected that the M-MCPD will have a shorter t_{rr} because the reduction on injection efficiency in the anode, this reverse recovery time is at least 2 times longer (≅75ns) compared to the recovery time of the M-PiN using lifetime control. However, these results are extremely attractive and encouraging for developing and modeling optimized M-MCPDs for power electronic applications because the possibility to achieve the same reverse recovery time of about 75ns, the lifetime required for the M-PiN would be of the order of ≅0.1μs compared to 1μs used for the M-MCPD rectifier without the problems and additional processing associated with lifetime control.

The results obtained from the simulations were shown to be in close agreement with the measured data of a commercial ultrafast diode. As it is well know the lifetime controlled diodes show the large leakage than usual diodes. However, the simulated and measured leakage current of the lifetime controlled diode was smaller than that of simulated M-MCPD diodes. The explanation that seems most likely is that, because for the M-MCPD the difference between defect level and intrinsic level, *Et-Ei*, was set as Etrap=0V, generation lifetime can be compared with recombination lifetime. Thus, the M-MCPD behaves like as Gold-doped diodes. It is also pointed out that if the carrier lifetimes in the drift-region were non-uniform, by means of lifetime profiling approach the reverse characteristics of real devices using Pt doping could have a better fitted characteristics.

Comparisons between experimental and calculated results of turn-off current waveforms were not obtained. Nevertheless, the resistive switching test results from computer simulations serve to support the statements regarding the dynamic behavior of the Mosaic Contact P-i-N Diodes.

Ability to fully evaluate the Modified Mosaic Contact P-i-N Diode concepts that were found to be potential competitors to the conventional P-i-N rectifier can only be followed from the integration of the concepts in real silicon. It is expected that such experiments will be carried out in the near future.

The M-MCPD should of course developed further. The following is a list of task recommended as continuation of the work reported in this thesis:

1) This thesis has dealt with a P^+/N^+ mosaic pattern. Considerable opportunities exist to propose and experiment with the structure showed in *figure* 5.1. A modification of the P^+/N^+ contact that achieves the same purpose is the substitution of the N^+ regions with a Schottky contact. It means a P^+/Schottky mosaic structure in which the Schottky junction is made between contact metal and a diffused P-region. Thus, varying the doping of the P^- region and the Schottky-contact region was found to be more effective in controlling the electrical characteristics.

2) During the operation of power devices, the device temperature is usually higher than the ambient temperature because of the power dissipation. The characteristics of these devices at high temperatures need to be investigated.

3) At high current levels lattice self heating leads to a significant current degradation, if the heat removal is poor. Therefore, from a modeling point of view, hydrodynamic transport model is extensively recommended to be taken into account carriers heating within the power device simulations.

Chapter 5

Conclusions and Future Work

A review of the literature on power rectifier diodes in silicon process showed that the availability of high-speed, high voltage (100V-600V) rectifiers, which match the performance of the new transistor such as the MOSFET or the IGBT, will aid the trend toward increasing circuit operating frequency. Thus the slow evolutionary progress in improving the performance of the P-i-N rectifiers in the past has been replaced by the introduction of several new devices concepts that can be expected to have a strong impact on power systems.

In this research work, a fast recovery epitaxial diode called Modified Mosaic Contact P-i-N Diode (M-MCPD) based on the anode injection efficiency control concept has been proposed. The M-MCPD consists of a lightly doped N-type epitaxial layer between the N^+ substrate (conventional epitaxial process) and a diffused P-region where the anode mosaic contact is placed. The P^+/N^+ mosaic contact is formed on the anode's surface by selective phosphorus and boron diffusion through its corresponding oxide mask.

Because of the aimed Computer-Aided Design approach, a Technology Computer Aided Design (TCAD) design methodology that employs 2-D technological, electrical and mixed-mode (circuit/device) simulators to develop and to optimize power rectifier diodes was presented. Although the focus is on power rectifiers, it is suggested that this approach will also aid in the speedy development of accurate physically-based circuit simulation models for complex power semiconductor devices structures.

Simulation of devices fabrication process and electrical behavior allows the investigation of all aspects of production prior to actual fabrication with the goal of design for manufacturability. Simulation allows qualitative and quantitative analysis of devices cross-section and circuit *a priori* in an effort to uncover otherwise inaccessible quantities such as carrier doping concentrations, electrostatic potential and electric field distribution. One of the most important advantages of TCAD is its predictive capability. Therefore, the use of these tools requires very good physical background knowledge as well as the support from the vendor.

The influence of variations in base lifetime on the rectifier characteristics has been examined from the standpoint of forward voltage drop at a given current and the leakage current at a given blocking voltage.

It was shown that the forward and reverse *I-V* characteristics of the M-MCPD are not quite affected by different mosaic area ratios. Furthermore, it was demonstrated that changes in the relative area of the N^+ mosaic region and the P^+ mosaic region in an M-MCPD rectifier can be used to control its switching characteristics in a similar manner to variations of the minority carrier lifetime by means of lifetime control used in conventional P-i-N rectifiers.

Thus, based on the simulation results, the M-MCPD rectifier were found to exhibit a better trade-off between forward drop and switching characteristics compared to its conventional counterpart, the modified P-i-N rectifier (M-PiN) with the conventional contact P^+ to the diffused P^- region.

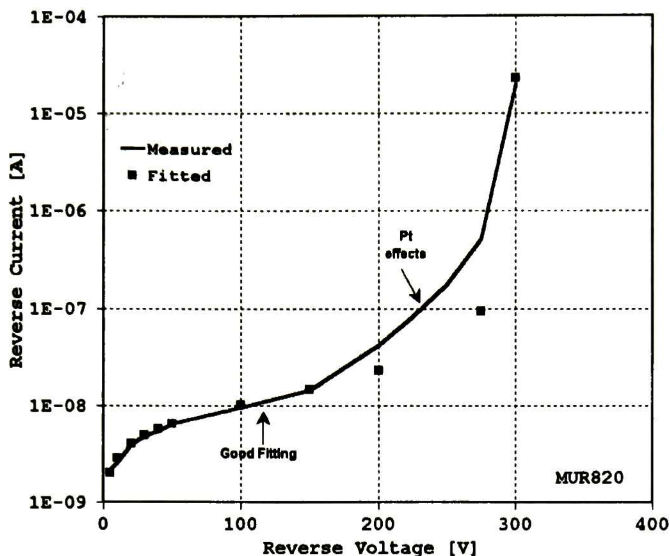


Figure 4.32: *Measured and fitted reverse I-V characteristics of the* MUR820 *ultrafast rectifier.*

Additionally, as mentioned in section 4.5, further investigations to demonstrate the actual position of recombination trap levels and their effects on the generation lifetime are necessary. Even though the statements discussed above, the obtained results using the TCAD tools may give suitable trends of the targeted specifications.

Unfortunately, a comparison of the reverse recovery current waveforms was not obtained. However, the computer simulation results serve to support the statements regarding the dynamic behavior of FRED devices. The results also provide a better understanding of the reverse recovery characteristics.

Table 4.6: *Regression coefficients calculated for regression equation (4.17)*

Device	n	I_S	R_S [mΩ]	B [V]	Range [V]
MUR820	2.0	1.10E-06	9.4	0.0527	0.500-1.2
M-PiN	2.1	9.90E-07	4.7	0.0535	0.540-1.2
M-MCPD	1.3	6.10E-10	9	0.0349	0.480-1.0

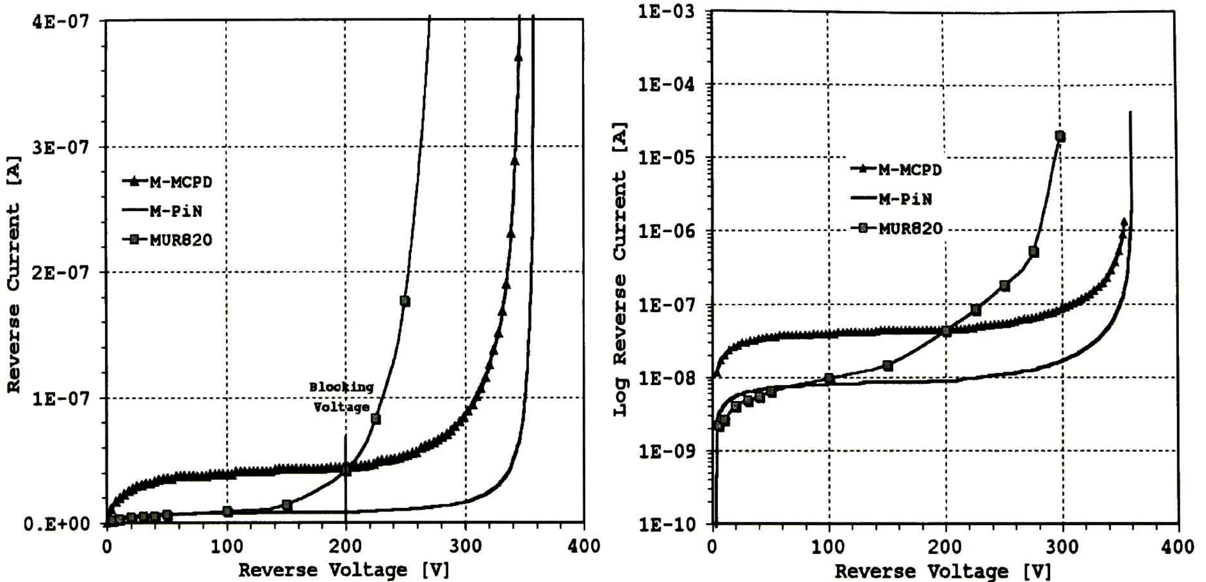


Figure 4.31: *Experimental off-state I-V characteristic of a commercial device,* MUR820, *compared with simulated ones.*

The measured reverse voltage across the diode compared with simulated ones is plotted in *Figure* 4.31. It should pointed out that the M-PiN and the M-MCPD rectifiers shows improved breakdown voltage. Unfortunately a conventional P-i-N diode without Pt doping was not available to be measured. Although the MUR820 rectifier shows a low level leakage current (as expected because of the Pt doping), the blocking voltage seems to be quite marginal according to the minimum specification value of 200V.

Table 4.7 shows the fitting coefficients estimated from expression (4.13), $I=I_S V^n M(BV_{PT}, V)$. *Figure* 4.32 shows fitted reverse *I-V* characteristics of the MUR820. As it can be seen, the fitting is very nice at low voltages. The explanation that seems most likely is that, since the heavy metal is diffused into the device, the measured Platinum doped rectifier have two lifetime regions. One close to the P^+-N^- junction, and another close to the N^+-N^- junction. The first one dominates leakage behavior at relatively low voltages, the second one impacts the breakdown voltage, and possibly t_{rr} behavior. Breakdown ionization coefficients cause relatively low *m* values. It is possible that a lifetime profiling approach could fit the reverse characteristics of real devices using Pt doping, it means non-constant drift-region lifetime.

Table 4.7: *I-V curve fitting coefficients including experimental data.*

Device	I_S	n	m	BV	τ_{SC}
MUR820	0.898pF	0.5	2	300V	4.63μs
M-PiN	1.9pA	0.299	5	360.5V	6.45μs
M-MCPD	8.0pA	0.33	5.5	355.5V	1.53μs

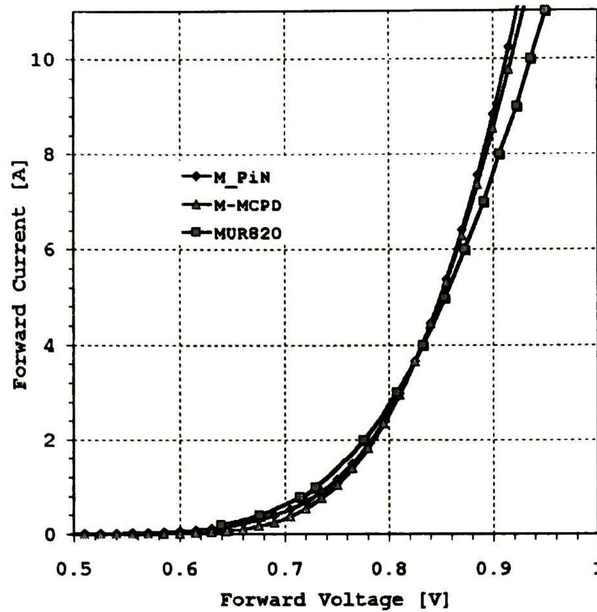


Figure 4.30: *Experimental on-state I-V characteristic of a commercial device,* MUR820, *compared with simulated ones.*

Both DC sweep an reverse measurements have been performed on the device. In these measurements, a high power pulse generator MASTEK was used for their adequate current range. Therefore, the results of the experimental data have been compared with numerical device simulations obtained by ISE-TCAD. First, the forward voltage behavior is analyzed. Typical forward *I-V* characteristic of the MUR820 measured at room temperature (pulse test: pulse width=300μs, duty cycle≤2.0%) is shown in *figure* 4.30 compared to the simulation results of the M-PiN and the M-MCPD (1P:3N) when the minority carrier lifetime is 50ns and 1μs, respectively.

To take into account the real parameters of the diode, a correction on equation (4.4) is made, by replacing the applied voltage V by (V-IR_S), where R_S is the series resistance of the diode. I_S, R_S and n are extracted from the current voltage characteristics. So equation (4.4) becomes

$$I = I_s \exp\left(V - IR_S \big/ nVt \right) \tag{4.16}$$

Based on equation (4.16), measured and simulated forward *I-V* characteristics were fitted, by means of a multiple regression method (JMP), to an equation of the type

$$V = \frac{nkT}{q}\ln(I) - \frac{nkT}{q}\ln(I_S) + IR_S \;=\; B\ln(I) + A + Im \tag{4.17}$$

The value of the main regression coefficients are reported in Table 4.6. The MUR820 rectifier shows normal ideality factor of 2 and a standard saturation current value. The *I-V* characteristics measured using a pulse test method can be used as reference for comparison purposes with simulated devices. Main differences between commercial device and the simulated ones are mainly due to the ohmic contact drops and bonding wires, modeled as a series resistances effects and lower saturation currents for simulated devices. Nevertheless with these effects taken into account, the results obtained with ISE-TCAD model show good agreement with experimental data.

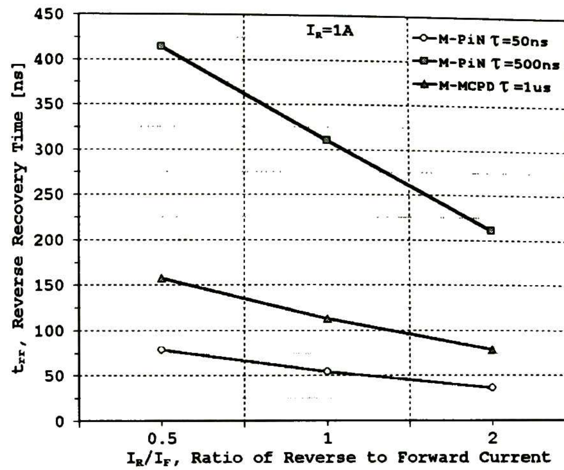


Figure 4.29: *t_{rr} vs. I_R/I_F of two M-PiN diode with $\tau_{n,p}$=500ns and $\tau_{n,p}$=50ns, and the M-MCPD 75% N^+ with $\tau_{n,p}$=1µs.*

Now it is important to compare the performance of the fastest M-MCPD, 75% N^+, to that of the M-PiN rectifier using lifetime variation. This comparison is provided in *figure* 4.27. It can be seen that reverse recovery time of the M-MCPD-75% N^+ is less than 80ns compared to the 215ns for the M-PiN using carrier lifetime of 500ns. However, considering the M-PiN rectifier using $\tau_{n,p}$=50ns for comparison, the reverse recovery time obtained for the M-MCPD is about 2 times longer than that for the M-PiN rectifier, t_{rr}=37ns, on which Pt doping was assumed.

Figure 4.28 illustrates the impact of lifetime variation on the excess-carrier concentration for the M-PiN compared to the M-MCPD. It is seen from *Figure* 4.28 that, a considerable reduction in the storage charge is presented in the M-PiN rectifies, as predicted by equation (4.2), where $\tau_{n,p}$ is directly proportional to the average injected electron/hole concentration in the drift-region $\bar{n}$. This result is also consistent with equation (4.15), where t_s, and hence t_{rr} are functions of minority carrier lifetime.

Since $t_{rr}=t_s+t_r$, qualitative agreement of t_{rr} data with relation (4.15), can be checked by plotting trr vs. I_R/I_F for any given diode, *Figure* 4.29 shows t_{rr} vs. I_R/I_F data taken from switching transient simulations of the M-MCPD and two M-PiN structures using $\tau_{n,p}$=500ns and $\tau_{n,p}$=50ns. This plot is often presented in diode specification data sheets.

Although the M-MCPDs reverse recovery behavior is still not as fast as that of the M-PiN assuming lifetime killing, the expected performances are extremely attractive and encouraging for developing and modeling optimized M-MCPDs for power electronic applications. For example, if an extrapolation of the results presented in *figure* 4.27 and *figure* 4.29 is made, it is possible to state that: to achieve the same reverse recovery time of about 75ns, the lifetime required for the M-PiN would be of the order of ≅0.1µs compared to 1µs used for the M-MCPD rectifier without the problems and additional processing associated with lifetime control. Thus a significant reduction in the drift-region lifetime in the M-PiN rectifier is required to achieve the same short reverse recovery time observed in the anode injection efficiency control rectifiers.

4.7. Model Validation With Commercial Diodes

Because of the aimed Computer-Aided Design approach, as an effort to validate the device models described in previous sections, measurements obtained by using a commercially available 200V, 8A ultrafast rectifier, MUR820 from Intersil (see appendix D) will be compared in the following paragraphs.

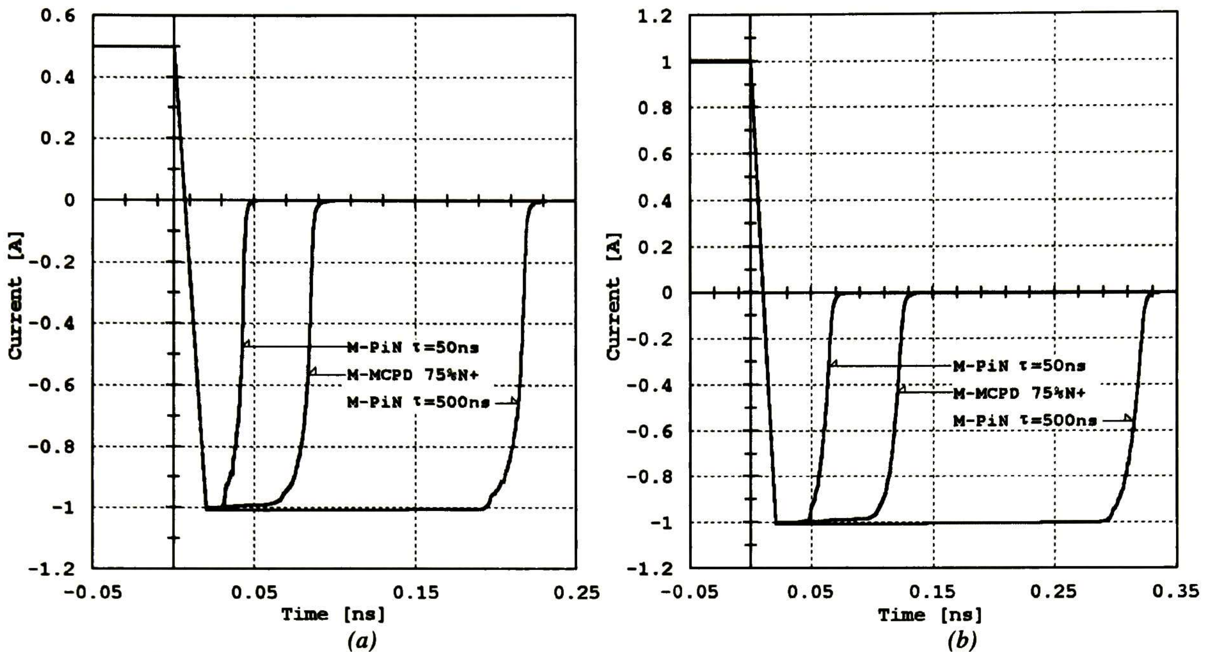


Figure 4.27: *Comparisons of reverse recovery current waveforms among the M-MCPD for the mosaic area ratio variants. (a)I_F=0.5A, I_R=1A; (b) I_F=1A, I_R=1A.*

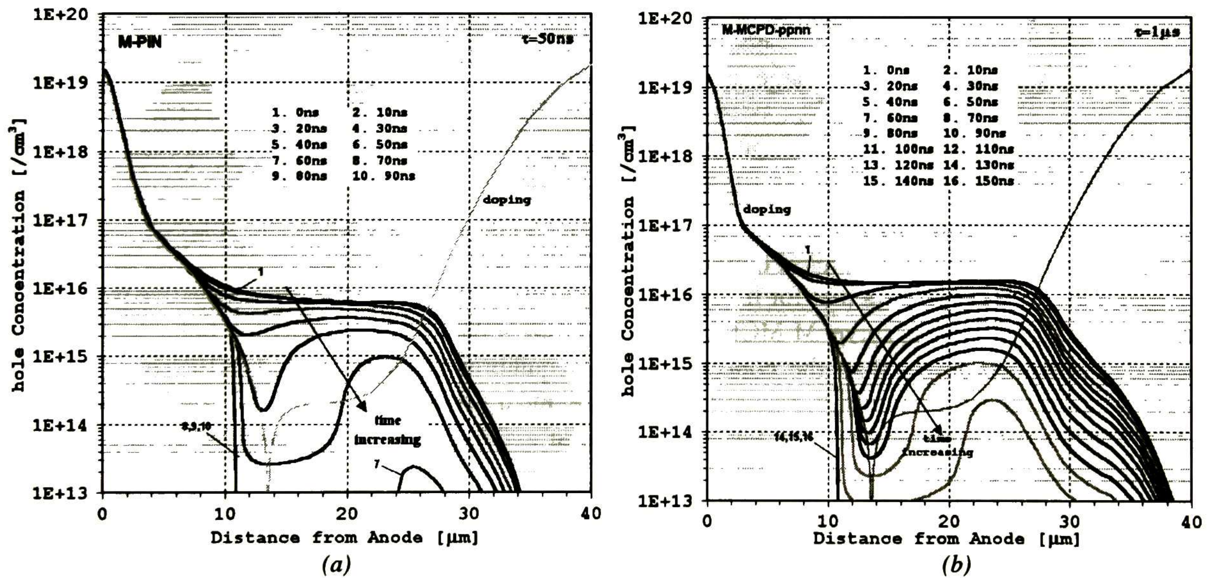


Figure 4.28: *Distribution of excess-carrier concentration in drift-region at different instant times in the reverse recovery transient shown in figure 4.27(b).(a) M-PiN using $\tau_{n,p}$=50ns. (b)M-MCPD-ppnn using $\tau_{n,p}$=1μs.*

As discussed earlier in section 4.4, the explanation that seems most likely is that less holes are injected from right hand side and the electron concentration must drop to maintain quasi-neutrality in the steady-state, e.g., at $t \leq 0$ns. This is the basic concept of anode injection efficiency control.

These results confirm the lower anode injection efficiency and hence the smaller stored charge in the M-MCPD rectifier that was indicated by the simulated carrier profiles.

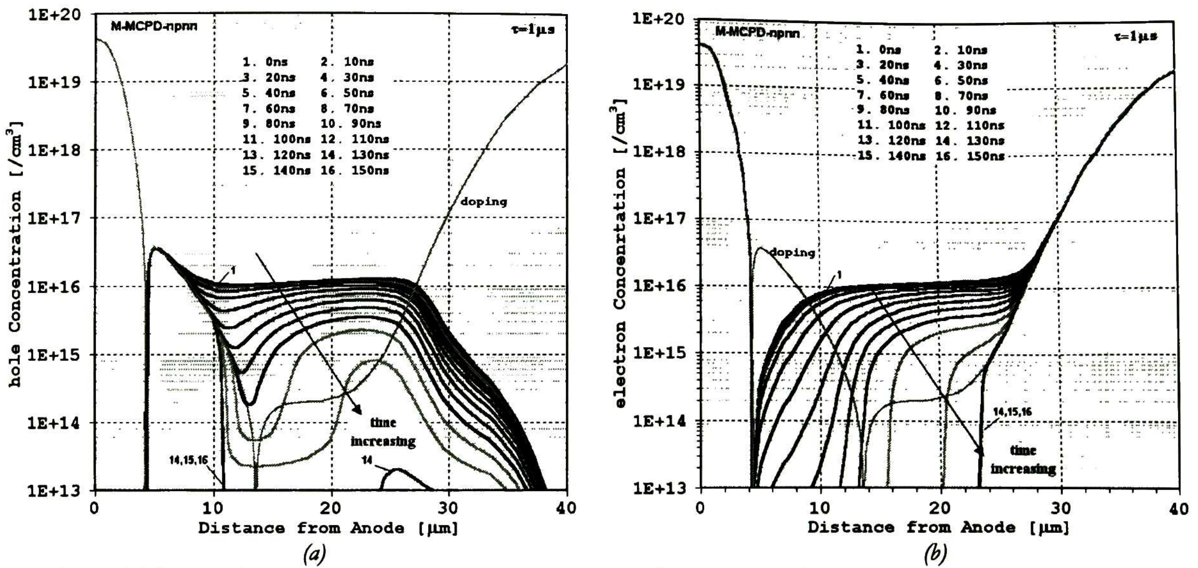


Figure 4.26: *Distribution of excess-carrier concentration in drift-region at different instant times in the reverse recovery transient shown in figure 4.22(b) of the M-MCPD-npnn rectifiers using* $\tau_{n,p}=1\,\mu s$.

The switching process for both rectifiers involves sweeping out of the charge carriers from both the P-N$^-$ junction and N$^-$-N$^+$ junction due to the high level injection conditions in the drift-region during the on-state. It can be notice that the reduction in the minority carrier concentration near the P-N$^-$ is more rapid when compared with the other end, the N$^-$-N$^+$. This asymmetry is a result of the unequal carrier mobilities. As mentioned in section 2.4.1, when $n(x)\cong p(x)$ is no longer fulfilled, a space charge is built up from *movable* charge carriers that an electric field starts to form in the lightly doped layer. This electric field will in turn assist in the sweep-out process of the stored carriers. Finally, the drift-region is completely depleted of mobile carriers approaching the reverse basing steady-state while the current continues to drop to its leakage level.

It is known that, in the current recovery time technique, t_S ends when the space charge region (SRC) is restored at the metallurgical boundary of P-N junction. Comparisons of the carrier distribution in *figure* 4.25(a) and (b) shows that for the M-MCPD structure at t=80ns, when the "negative step" on I_R dependence is over (see curve M-MCPD 75% in *Figure* 4.22(b)), the density of holes at the P-N$^-$ boundary becomes lower than the concentration of equilibrium electrons, N_D=2x10^{14}cm^{-3}. Just this moment corresponds to the SCR restoration at the boundary and decrease of the reverse current. For M-PiN structures, quasi-neutrality is fully maintained at t=80ns. Only at $t\cong$430ns the density of holes becomes lower than N_D.

Hence, increasing the proportion of the N$^+$ mosaic region was found to reduce the amount of carriers stored device drift-region. This in turn reduces the reverse recovery time in the M-MCPD as the N$^+$ mosaic region increases. Based on the above discussion, better switching performance can be obtained for the M-MCPD rectifier by changing the geometrical parameters of the mosaic contact. Thus changes in the relative area of the N$^+$ mosaic region and the P$^+$ mosaic region in an M-MCPD rectifier can be used to control its switching characteristics in a similar manner to variations of the minority carrier lifetime used in the conventional P-i-N rectifiers by means of Platinum diffusion.

The reduction in the reverse recovery time is mainly due to the fact that the M-MCPD rectifier has a smaller stored charge in the drift-region compared to the M-PiN rectifier; see *figure* 4.25.

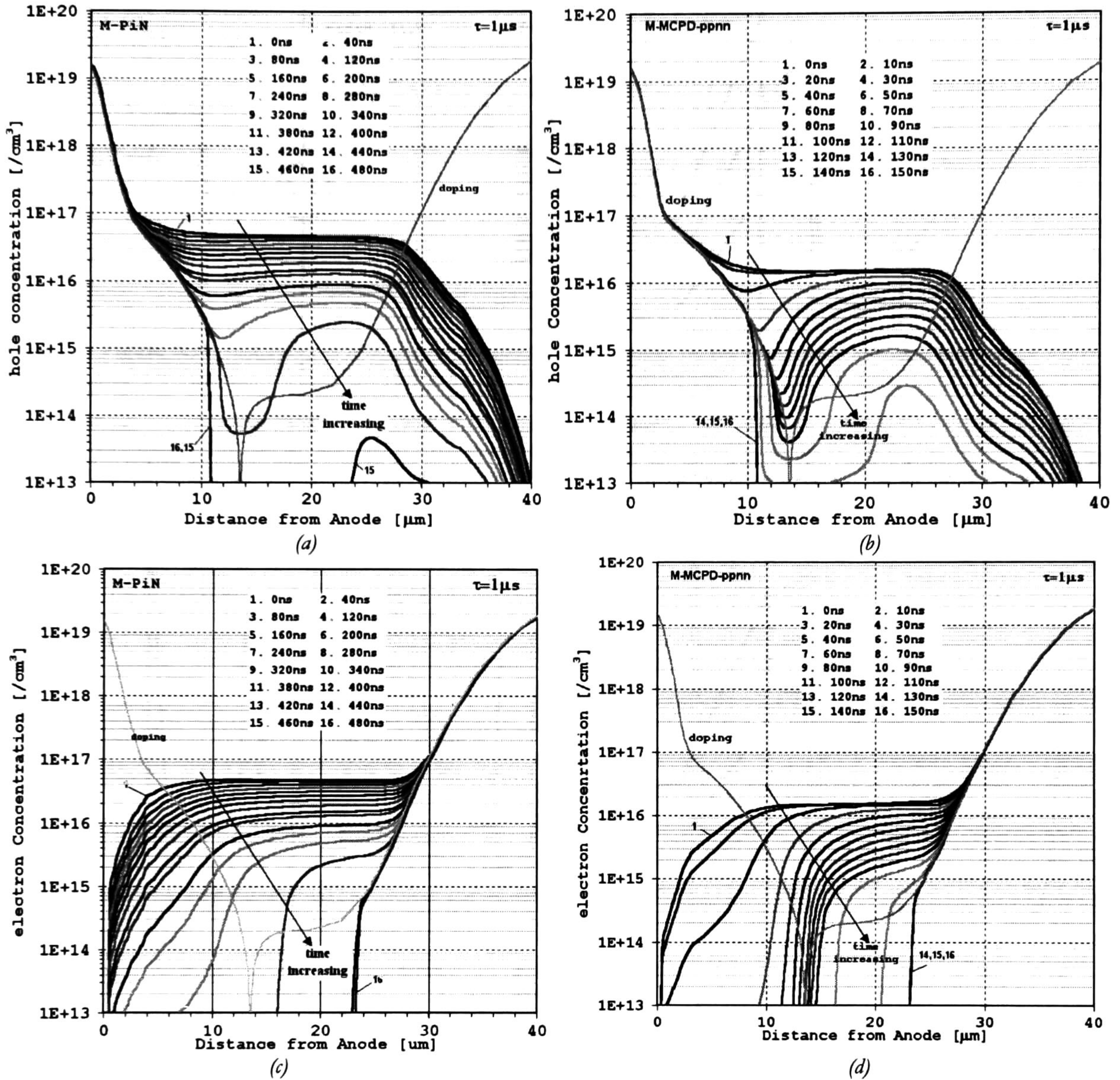


Figure 4.25: *Distribution of excess-carrier concentration in the drift-region at different instant times in the reverse recovery transient shown in figure 4.22(b) of the M-PiN and M-MCPD-ppnn rectifiers using* $\tau_{n,p}=1\,\mu s$.

It should be noted that in this model the lifetime τ is not directly linked to any physical parameter like carrier lifetime, transit time or carrier density so it is an "effective" lifetime. However τ is sometimes used as $\tau=\tau_{n,p}$. Considering the M-MCPD rectifier with 50% N+ mosaic region for comparison in *figures* 4.23 and 4.24, the reverse recovery time obtained for the M-MCPD is at least approximately 3 times shorter than that for the M-PiN rectifier.

In order to get an insight of the device behavior during the turn-off transient that could allow to understand the causes of the onset of reduction in t_{rr} and to design the best diode structure for improving it, the excess carrier distribution for the rectifiers through the P+ region (M-MCPD with 75% N+ area) at different time instants in *figure* 4.22(b), are compared in *figure* 4.25. *Figure* 4.26 shows the carrier distribution in the M-MCPD *npnn*-section.

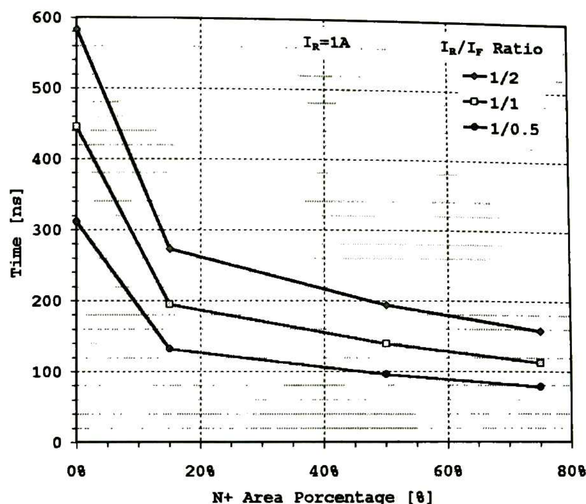


Figure 4.23: *Simulated reverse recovery time as a function of percentage of N^+ mosaic area. The minority carrier lifetime was 1μs in all the cases. The point at 0% N^+ mosaic area represents an M-PiN rectifier. I_R was held constant at 1A while I_F was varied.*

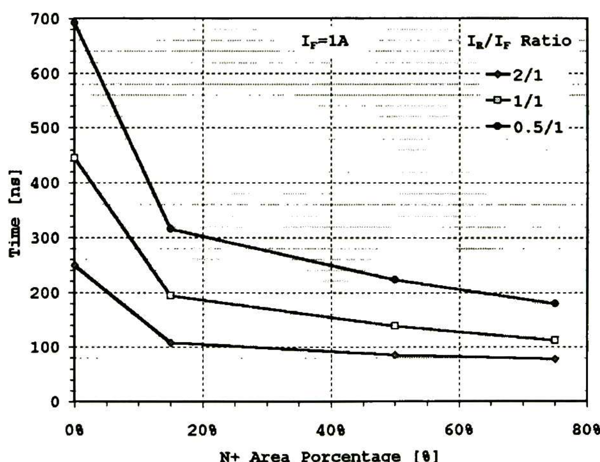


Figure 4.24: *Simulated reverse recovery time as a function of percentage of N^+ mosaic area. The minority carrier lifetime was 1μs in all the cases. The point at 0% N^+ mosaic area represents an M-PiN rectifier. I_F was held constant at 1A while I_R was varied.*

For *Figure* 4.23, I_R is held constant while I_F is varied. The storage charge increases as I_F increases, consistent with the fact that it takes longer for the increasing number of carriers injected at higher levels of I_F to recombine. *Figure* 4.24 shows the general effect of holding I_F constant while varying I_R. As increased I_R permits quicker diffusion current removal of excess-carrier during the switching transient leading to a decrease in t_s and hence in t_{rr}. This storage charge is the time necessary for the excess-carrier concentration at the edge of the transition region to go to zero. The reverse recovery switching transients are consistent with classical silicon diode behavior as dictated by [40]

$$t_s = \tau \cdot \left\{ erf^{-1}\left[1 + \frac{1}{I_R/I_F} \right] \right\}^2 \tag{4.15}$$

This formula is based on the charge control model [29].

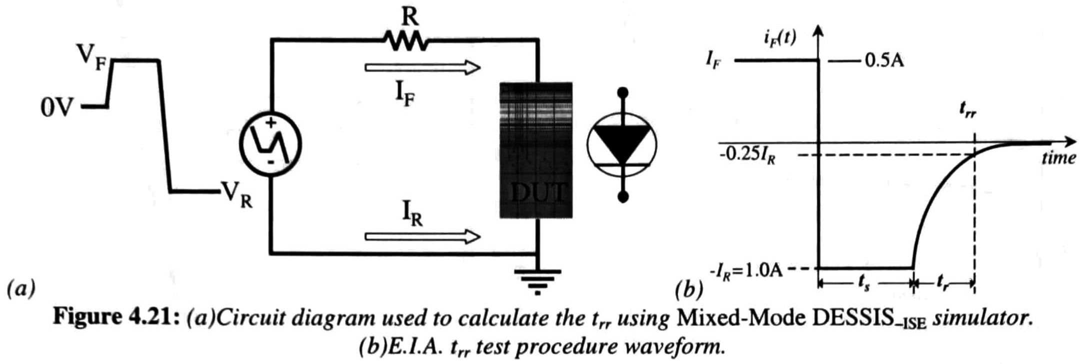


Figure 4.21: *(a)Circuit diagram used to calculate the t_{rr} using* Mixed-Mode DESSIS$_{-ISE}$ *simulator. (b)E.I.A. t_{rr} test procedure waveform.*

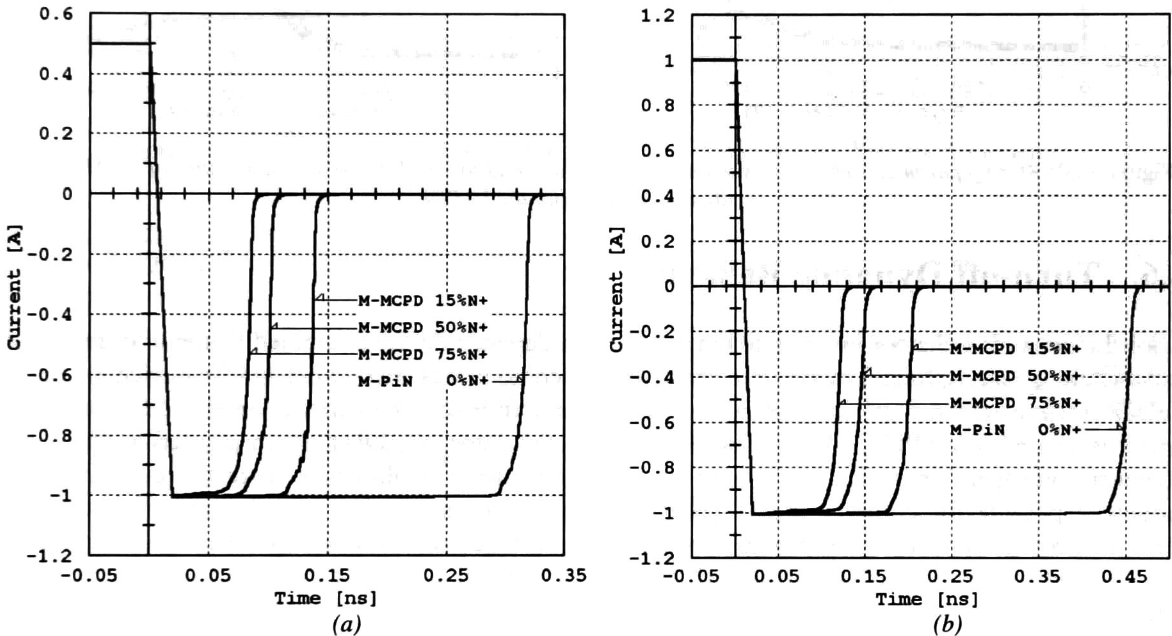


Figure 4.22: *Comparisons of reverse recovery current waveforms among the M-MCPD for the mosaic area ratio variants. (a)I_F=0.5A, I_R=1A; (b) I_F=1A, I_R=1A.*

From these results is evident why conventional P-i-N diodes require the introduction of heavy metals to optimize the dynamic device behavior. On the other hand, introduction of heavy metals requires diffusion at elevated temperatures (above 700°C) before completion of the device fabrication. These metals are fast diffusing, making it difficult to control the final defect distribution and cross-contamination in the production line is a constant risk. This technological drawback is one of the main reasons for which use Gold or Platinum doping used as method of carrier lifetime control is being eliminated.

The variation of the reverse recovery time as a function of percentage N^+ mosaic area for varying I_F and I_R are plotted in *figure* 4.23 and *figure* 4.24. Three ratios of reverse to forward current I_R/I_F were simulated: 2, 1 and 0.5.

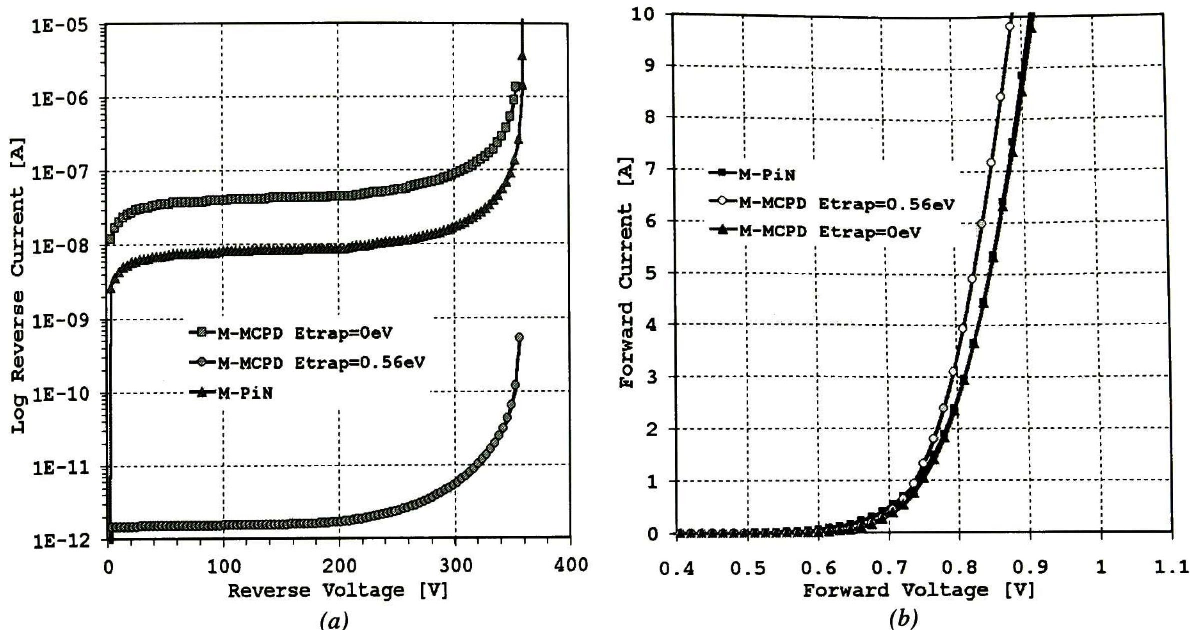


Figure 4.20: Etrap *parameter effects on simulated reverse (a); and forward (b) I-V characteristics of the M-MCPD rectifier compared with the M-PiN.*

4.6. Turn-off Dynamic Behavior

Since the dynamic behavior investigated in this section depends on the combined features of the FRED and switching circuit, mixed-mode (circuit/devices) technique was used, whereby the device under test (DUT) is simulated using a finite-element method and drift-diffusion model, while the surrounding circuit is treated in a SPICE-like fashion. In a circuit simulator, the DUT is represented in terms of a compact equivalent circuit model. It is often difficult to develop physically correct circuit simulation models, especially for complex power semiconductor device structures. Mixed simulations can thus serve to provide the necessary physical insights that will help to develop accurate circuit simulation models. This technique also provides access to internal carrier dynamics of the device when subjected to actual stresses relevant to the end application. Hence, an accurate physically based circuit simulation model accounting for all application stresses can be developed using the proposed technique.

For the sake of numerical convergence, the turn-off under a resistive load was simulated using the circuit shown in *figure* 4.21. The circuit used in the simulations is simpler than that used in the measurements, but it retains the essential feature. The step reverse recovery method is the Electronics Industries Associations -E.I.A.- test procedure [41]. DUTs were switched from an on-state condition, while carrying a forward current I_F, to an off-state condition. A time dependent voltage source through a piecewise linear function was used to control the reverse current I_R. The reverse recovery time t_{rr} can then obtained from the current waveform outlined in *figure* 4.21.

It should be notice that the M-PiN rectifier represents the zero mosaic area ratio, it means L_{P+}=60μm, L_{N+}=0μm (4P:0N) or 0% N^+ contact region. Thus, the 3P:1N, 1P:1N and 1P:3N area ratios represent the 25%, 50% and 75% of the N^+ mosaic contact region, respectively. Simulated waveforms of the M-MCPD reverse recovery current, with its "four" mosaic area ratio variants are shown in *figure* 4.22 using a minority carrier lifetime of 1μs. Transients have been shifted horizontally for clarity. The reverse recovery times for the M-MCPD rectifiers are less than 135ns (largest t_{rr}) compared to the 300ns for the M-PiN rectifier.

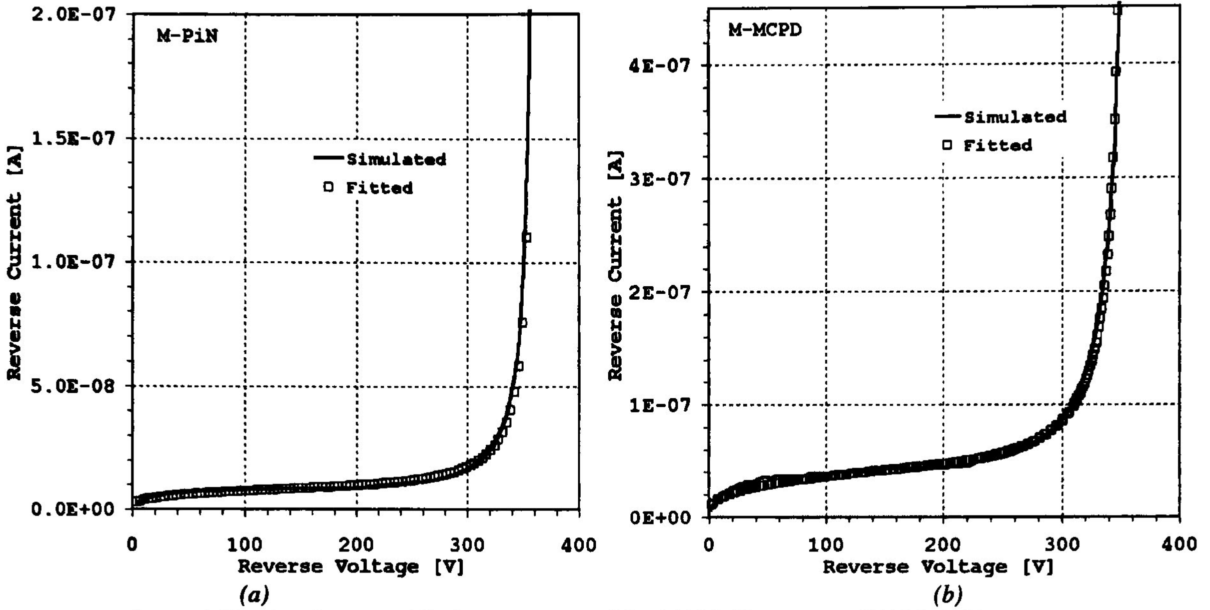


Figure 4.19: *Fitted reverse I-V characteristics of the (a)M-PiN structure; (b)M-MCPD structure.*

$$M = \frac{1}{\left[1-\left(V/BV_{PT}\right)^{m}\right]} \tag{4.14}$$

where m is between $3 \leq m \leq 6$ and $V^{n} \propto W_{SC}$. Simulated *I-V* characteristics of both M-PiN and M-MCPD devices were fitted using this approach; see *figure* 4.19. Both devices showed standard fitting coefficients for normal P-N junctions; see Table 4.5. Lifetime values of simulated devices are of the order of magnitude of the proposed lifetimes, $\tau_{n,p}$=50ns and $\tau_{n,p}$=1μs.

Table 4.5: *I-V curve fitting coefficients.*

Device	I_S	n	m	BV	τ_{SC}
M-PiN	1.9pA	0.299	5	360.5V	6.45μs
M-MCPD	8.0pA	0.33	5.5	355.5V	1.53μs

Since for the M-MCPD the difference between defect level and intrinsic level, *Et-Ei*, was set as `Etrap` =0V, generation lifetime can be compared with recombination lifetime. Thus, the M-MCPD behaves like as Gold-doped diodes, which have their dominant recombination level in silicon close to the intrinsic level. Now, if the activation energy were set to 1.12eV, being equal to the silicon bangap, then `Etrap`=1.12eV-0.56eV=0.56eV. *Figure* 4.20(a) and (b) show the `Etrap` parameter effects on simulated reverse and forward *I-V* characteristics of the M-MCPD rectifier compared with the M-PiN. It can been seen that both reverse and forward characteristics present improved performance. Therefore, further investigation is necessary to demonstrate the feasibility of this approach.

Equation (4.12) has important device design implications. By choosing a recombination center with the appropriate energy level, τ_{SC} can be made much higher than $\tau_{n,p}$. Hence a device which depends on $\tau_{n,p}$, e.g., the turn-off time, can be varied independently from a device property that depends on τ_{SC}, e.g., diode leakage current. From the analysis of results presented above, it is important to recall that in the space-charge region of a reverse-biased device one cannot speak of minority carrier lifetime.

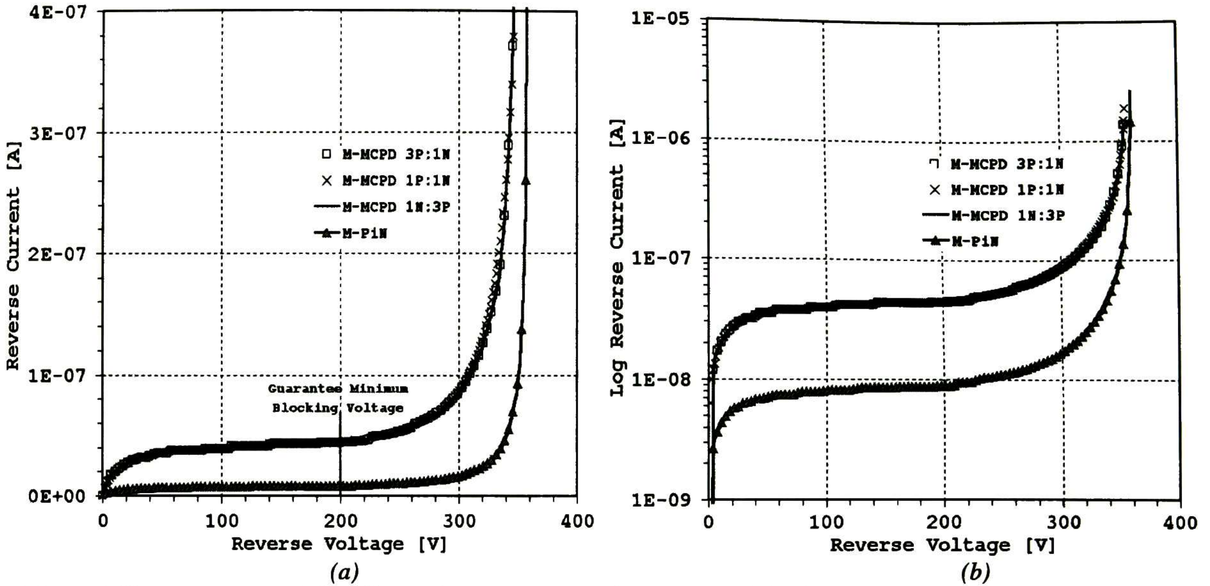


Figure 4.18: *Comparison of the off-sate characteristics of the M-PiN and the three mosaic variants of the M-MCPD. (a)Lineal scale; (b)semi-logarithmic scale. The minimum reverse blocking voltage is guaranteed for all structures.*

where A is the diode area and n_i the intrinsic carrier density. Thus a low leakage current is obtained when the space-charge generation lifetime τ_{SC} is large. But this tendency cannot be confirmed from *figure* 4.18 because the opposite is true, which owns its explanation to the following factor: the generation lifetime is sometimes referred to as the minority carrier generation lifetime, creating further confusion. τ_{SC} depends inversely on the impurity density and the capture cross section for electrons and holes (N_T, σ_n and σ_p), just as τ_{SC} does. In addition, however, it depends exponentially on the energy level E_T [7].

It has been shown that, τ_{SC} is much more sensitive to E_T and capture cross section than $\tau_{n,p}$ because electron-hole pair generation, being a thermally activated process, is very sensitive to the impurity energy level Recombination, on the other hand, is relatively insensitive to at least over the central portion of the bandgap, as illustrated in *figure* 1.3 in Chapter 1. The generation lifetime can be quite large if $E_T \neq E_i$, e.g., when the center is asymmetrical. If the σ_n and σ_p do not differ to greatly, by a factor of 100 or less, τ_{SC} can be written as [25]

$$\tau_{SC} \cong 2\tau_{n,p}\sqrt{\sigma_n / \sigma_n}\cosh\left[\left|E_T - E_i\right|/kT\right] \tag{4.12}$$

For example, recalling that E_T -E_i=-0.14V was set, τ_{SC} $\cong 200\tau_{n,p}\sqrt{\sigma_n / \sigma_n}$ Using Pt values for σ_n=3.2x10^{-14} and σ_p=2.70x10^{-12} [7], then τ_{SC} ≅1.2μs. To tackle the above issue, the following expression can be used to evaluate reverse I-V characteristics, knowing avalanche or punch-through voltage [35],

$$I \cong I_S V^n M(BV_{PT}, V) \tag{4.13}$$

where n is a coefficient that consider depletion space charge width variation with reverse-bias. The variation of the avalanche multiplication factor M as function of the applied reverse-bias voltage V is given by [35]

Table 4.4: *Final parameters of the M-MCPD2 and M-MCPD3 structures.*

Structure	Anode	N_B [cm^{-3}]	Epi-THK [µm]	Cs [cm^{-3}]	Xjn [µm]	Xjp [µm]	Subs-THK [µm]	Rho-Subs [Ω-cm]	Area [cm^2]
M-MCPD2	p-	2x10^{14}	42	**1.0x10^{18}**	-	13.5	345	0.00145	0.030
	p+			1.5x10^{19}	-	3.0			
	n+			4.5x10^{19}	4.5				
M-MCPD3	p-		48	**1.0x10^{16}**	-	13.5			
	p+			1.5x10^{19}	-	3.0			
	n+			4.5x10^{19}	4.5				

It can be seen from *figure* 4.16 that, as the impurity concentration in the P-N junction is increased, the depletion with W_{SC} decreases inversely as the square root of the impurity concentration as stated by eq. (4.9) [13] (see section 1.4.1),

$$W_{SC} = \sqrt{\frac{2\varepsilon_S}{q}\left(\frac{N_A + N_D}{N_D N_A}\right)(V_{bi} - BV)} \tag{4.9}$$

where ε_S is the dielectric constant for silicon, q the magnitude of electronic charge, N_A and N_D acceptor impurity density and donor impurity density, respectively. V_{bi} is the built-in potential and BV the breakdown voltage. With $N_A >> N_D$ and $BV >> V_{bi}$, eq. (4.10) becomes

$$W_{SC} = \sqrt{\frac{2\varepsilon_S BV}{qN_D}} \tag{4.10}$$

The potential is related to the field by $V = -\int E(x)dx$. Thus, the potentials are the areas under $E(x)$ curves shown in *figure* 4.16. Therefore, the lower the concentration of the diffused P^- region, the larger the breakdown voltage caused by the area of the electric field distribution; see *figure* 4.17.

Figure 4.18 compares the simulated reverse *I-V* characteristics of the three M-MCPD design variants, 3P:1N, 1P:1N and 1P:3N, for $\tau_{n,p}$=1µs and the M-PiN for $\tau_{n,p}$=50ns. It can be seen that both the M-MCPD and the M-PiN rectifiers can withstand reverse bias voltages of more than 350V at 25°C using the material parameters specified in Table 4.2, thus the minimum blocking voltage of 200V is guaranteed. The characteristics of the three M-MCPD design variants are practically indistinguishable. It can be concluded, at least under these two-dimensional simulation assumptions, that the breakdown voltage and the leakage current in the M-MCPD rectifier can not be controlled by varying the mosaic area ratio.

As well known the lifetime controlled diodes show the large leakage than usual diodes. However, from *figure* 4.18 it is evident that the simulated leakage current of the lifetime controlled diode is smaller (≅8.83nA) than that of M-MCPD diodes (≅44.4nA). Since all the possible failure mechanisms have as a consequence an increase of the leakage current with respect to the devices in non-stress conditions, the reduction of the leakage current is an important task [27]. The reduction of the leakage current is related inversely proportional to the model by the space-charge generation leakage current discussed in Chapter 1, section 1.4.2 as

$$I_S = {qAn_iW_{SC}}/{\tau_{SC}} \tag{4.11}$$

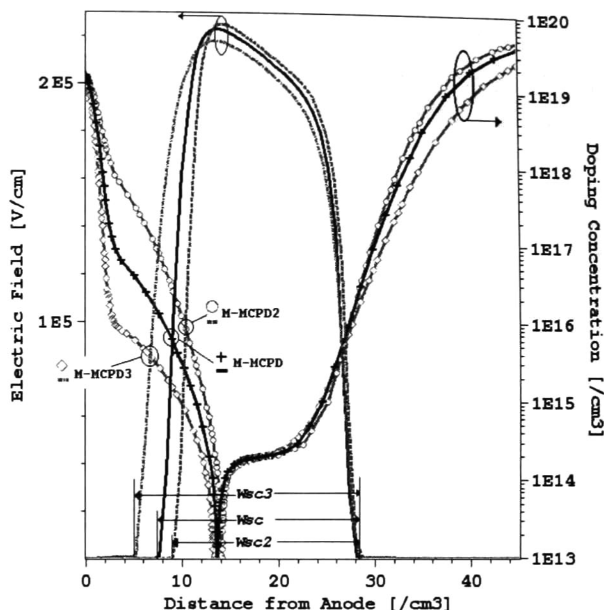


Figure 4.16: *Comparison of the doping and electric field profiles variants for the M-MCPD to show the impact upon the breakdown voltage.*

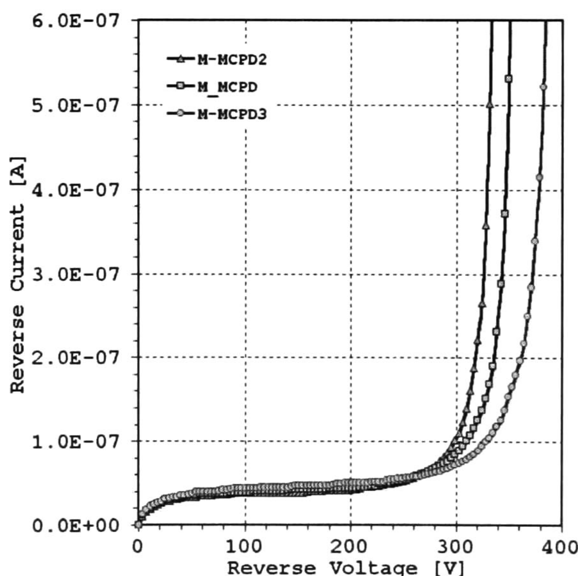
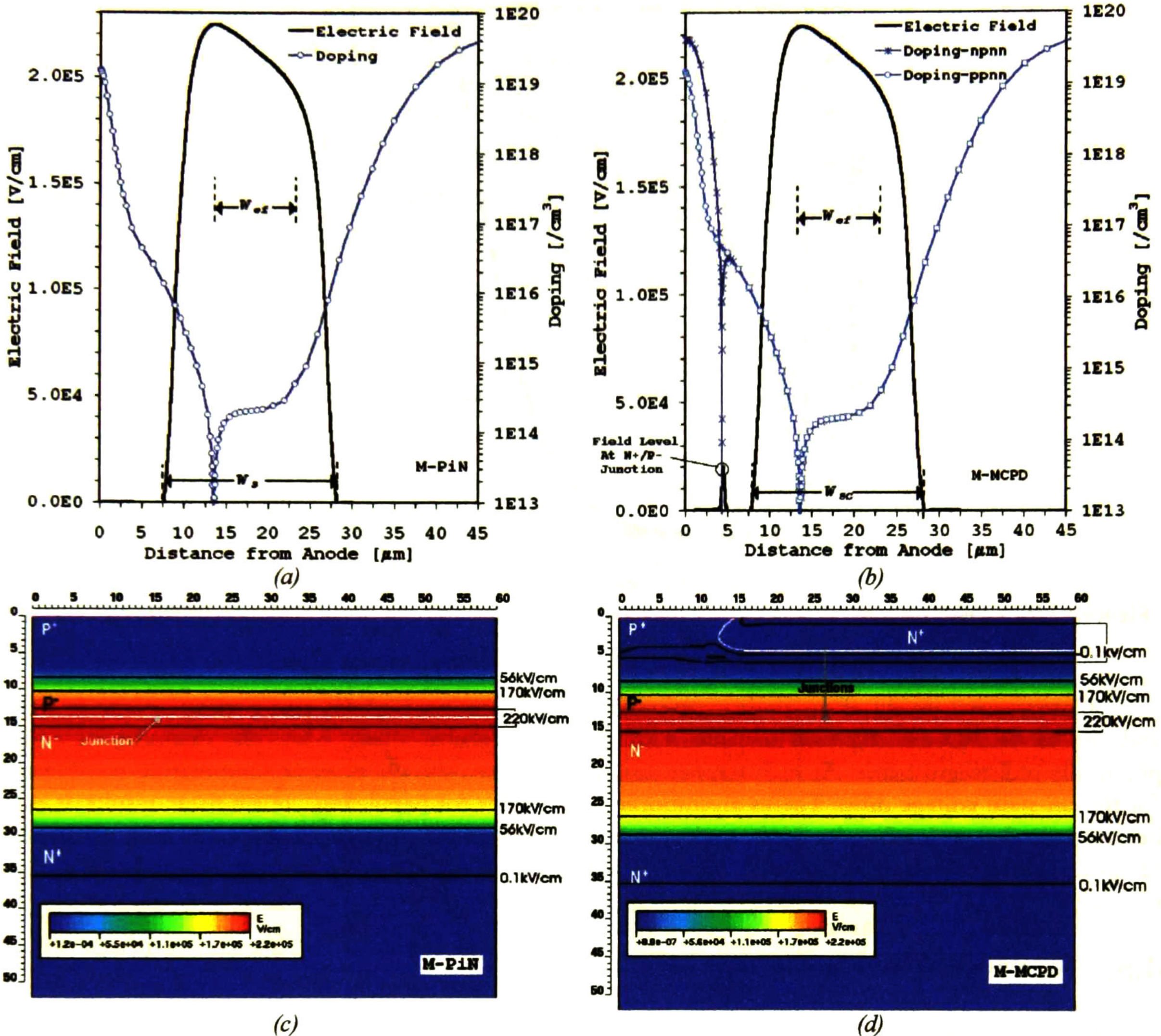


Figure 4.17: *Comparison of the reverse I-V characteristics of the M-MCPD structure with different surface concentration on the diffused P⁻ region.*

Figure 4.16 shows the doping profiles and electric field distributions of the M-MCPD along the *ppnn*-section. There different values ($1x10^{18}$, $1x10^{17}$ and $1x10^{16}cm^{-3}$) of surface concentration for the diffused P^- region were performed. Epitaxial layer thickness was adjusted to keep up junction depths consistent for each structure. The solid-state diffusion from the substrate to the epitaxial layer differs because different thermal treatments were applied. The reference structure is that presented in Table 4.2. Table 4.4 shows the final parameters of the M-MCPD2 and M-MCPD3 structures used for this analysis.



(a) (b)

(c) (d)

Figure 4.15: *(a) and (b)Resulting 1-D shape of electric field; and (c) and (d)distribution of equi-field lines, at breakdown voltage in the M-PiN with $\tau_{n,p}$=50ns and in the M-MCPD with $\tau_{n,p}$=1µs.*

$$E_{Max} = K \cdot N_B^{1/8} = 245\text{kV/cm} \qquad (4.8)$$

where N_B=doping of the middle layer (2x10^{14}); K=4010V·cm$^{-5/8}$, empirical constant.

Distribution maps of equi-field lines at breakdown voltage for both the M-PiN and M-MCPD rectifiers are shown in *Figure* 4.15(c) and (d). It can be seen that, the equi-field line intervals are practically equal in the drift-region for both structures. Notice that, since the field level in the forward-biased N^+-P^- junction in the mosaic contact is too small compared with E_{Max}, it does not breakdown by avalanche. Due to the non-uniformly doped distribution in the P^- region (and auto-doping effects), a compensation effect that reduces the electric field is caused and the depletion into the diffusion is not negligible. Then, the voltage is not supported exclusively by the lightly doped N-base. Therefore, making a proper adjustment of impurity concentration in the P^- region and the N-type layer, the suggested structures make possible to increase the blocking voltage without sacrificing the forward voltage.

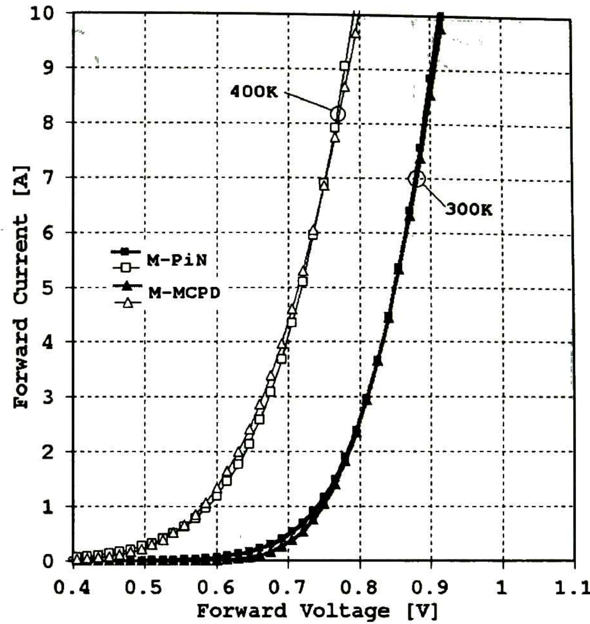


Figure 4.14: *Comparison of the forward I-V Characteristics of the M-PiN ($\tau_{n,p}$=50ns) and the M-MCPD ($\tau_{n,p}$=1μs) at T=300K and T=400K.*

Comparative results of the static characteristics performed at T=300K and T=400K of the M-PiN and the M-MCPD are depicted in *figure* 4.14. At 300K, above about 1.5A, the characteristics are practically indistinguishable. At high temperature both devices show a positive temperature coefficient for the on-state voltage drop. This is an important parameter for paralleling. Form these results, it can be conclude that, at least under these work simulation assumptions, the modified MCPD with no carrier lifetime control is in agreement with the M-PiN rectifier which uses lifetime control to achieve fast recovery.

4.5. Reverse Blocking Capability

In order to obtain the reverse *I-V* characteristics, it was necessary to connect a 100MΩ resistance at the substrate. Using a resistor at the substrate contact enables the simulation to increase the substrate voltage above the breakdown voltage, which results in large currents, otherwise convergence was a problem.

Figure 4.15(a) and (b) illustrate the resulting shape of electric field distribution and doping profile as a function of distance from anode's surface for both the M-PiN and M-MCPD (1P:3N) rectifiers with $\tau_{n,p}$=50ns and $\tau_{n,p}$=1μs, respectively. The "trapezoidal" shape of the electric field distribution profiles clearly show how punch-trough occurs before avalanche breakdown takes place. The effective width of the drift zone W_{neff} can be defined as the region between maximum electric field at both sides the P^--N^- junction and N^+-N^- junction. Space charge width saturates for epi-layer doping concentrations of the order of $10^{16}cm^{-3}$.

During the off-state, the peak electric field occurs at the P^--N^- junction as shown in *figure* 4.15(a) and (b). The maximum allowable value of electric field at which avalanche breakdown occurs is about E_{Max}=224kV/cm for both structures. In a practical sense, a "permissible operating voltage" maybe defined such that the electric field in the semiconductor body never exceeds a critical value. This is a very reasonable result and is in good agreement with the expression given by [14]

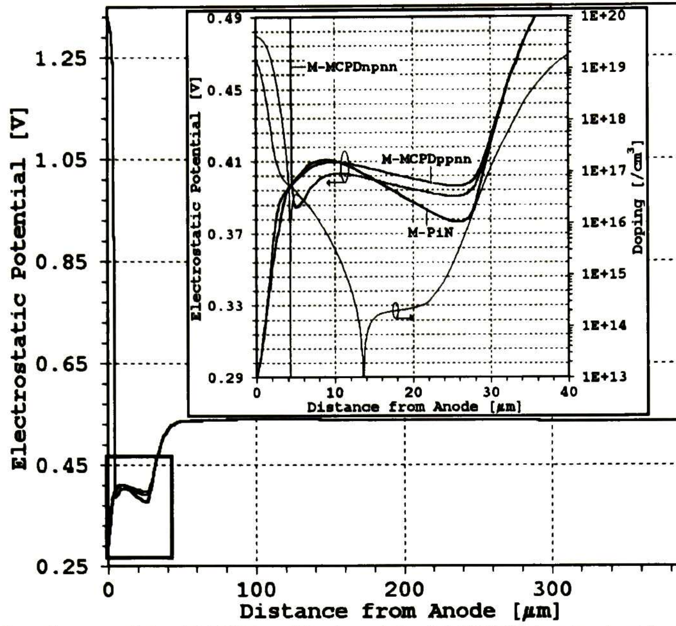


Figure 4.12: *Potential distribution of the M-PiN (τ=50ns) and the M-MCPD (τ=1μs) with an applied voltage of 0.8V.*

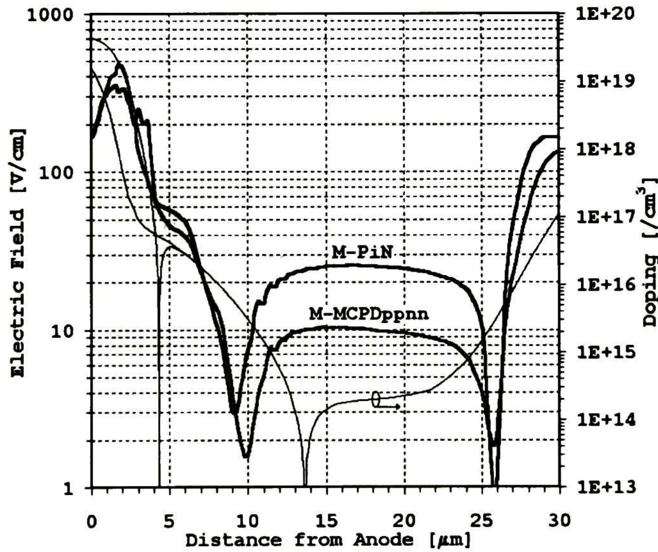


Figure 4.13: *Forward bias Electric Field distribution of the M-PiN (τ=50ns) and the M-MCPD ppnn-section (τ=1μs). Applied voltage equals to 0.8V.*

The difference between the drift-region voltages could be better appreciated with the aid of *figure* 4.13. This figure shows the doping profile and electric field distribution for an applied voltage of 0.8V in both rectifiers. The base voltage V_m can be approximated by [13]

$$V_m = E' \cdot W \tag{4.7}$$

where E' is the average electric field in the depletion region. Thus a lower electric field developed across middle region keeping the voltage across the diode small.

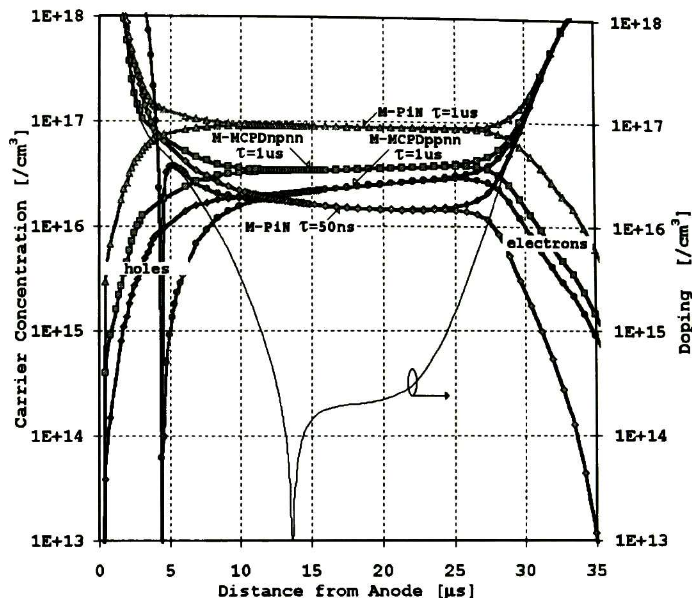


Figure 4.11: *Carrier distribution in the drift-region at 3A of the M-PiN (τ=50ns, 1μs) and M-MCPD (τ=1μs).*

In order to show the lifetime effect on the carrier concentration, *Figure* 4.11 shows the carrier distribution of both rectifiers at current of 3A. Compared with the drift-region background doping concentration of $2x10^{14}cm^{-3}$ it is clear that the conductivity modulation happened in the drift-region and the electron and hole concentrations became much larger than the native doping level. In order to keep the charge balance in the drift-region, the hole and electron concentrations are forced to be the same ($n(x)=p(x)$).

Notice that, in the mosaic structure, the carrier concentration in the steady-state is less than that of the non-mosaic structure for the case of the same carriers lifetime value, 1μs. This is because the width of the P^+-region was reduced (1P:3N or 75%), thus less holes are injected from the anode side and the electron concentration must drop to maintain quasi-neutrality. This reduced carrier concentration results in reduced stored charge.

The condition $d/L_a=1$, or $W=2L_a$, marks the transition between a "short" ($W \leq 2L_a$) and a "long" ($W>2L_a$) P-i-N diode. For the short structure, the spatial variation in carrier concentration over the drift-region has little effect on the voltage drop. For the long structure, the voltage drop across the drift-region can be quite high and may not be satisfactory. To maintain a short-structure characteristic, L_a must be large. At high injection conditions, the ambipolar diffusion coefficient D_a decreases with increasing injected carrier concentration because of carrier-carrier scattering effects. Therefore, L_a will decrease as current density increase, causing the ratio W/L_a to increase. The voltage drop across the diode is high when W/L_a is grater than 2; as a result, the diode current increases much more slowly with increasing applied biases, marking the "worsening" of the rectifier characteristics [13]. The condition $W>2L_a$ occurs at lower biases for rectifiers with shorter ambipolar carrier lifetime, which explain the crossover of the current curves for both the M-PiN and M-MCPD rectifiers, as shown in *figure* 4.10(a) and (b). It is noted that, the presence of the mosaic contact in the M-MCPD pushes the crossover point to lower current densities.

Figure 4.12 shows the electrostatic potential distribution along a vertical cut line of the rectifiers. As it can be seen, the forward voltage drop across the drift-region is smaller in the M-MCPD rectifier with $\tau_{n,p}$=1μs, assuming no lifetime killing, than in the M-PiN rectifier with $\tau_{n,p}$=50ns.

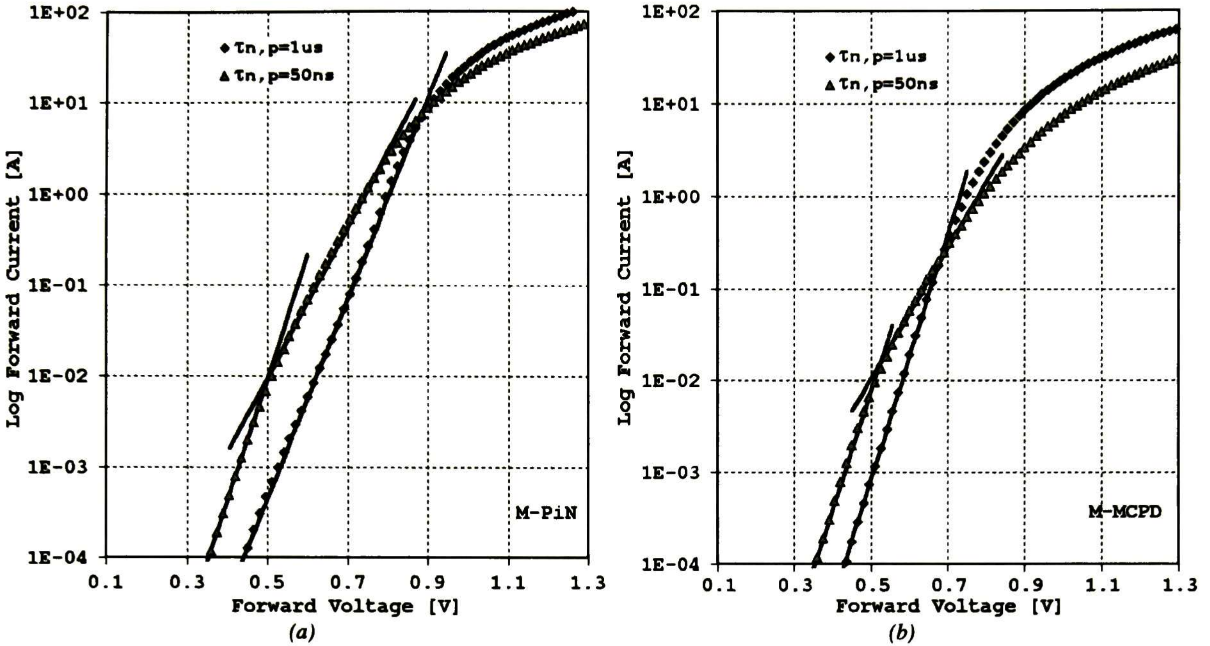


Figure 4.10: *I-V Characteristics as a function of the carriers lifetime. (a)M-PiN; (b) M-MCPD. The straight lines indicate the regions where I varies as exp(V/nVt).*

Finally, calculate values for the parameters from the following equations:

$$n = \frac{V_1 - V_2}{Vt \ln(I_1/I_2)} \qquad (4.5)$$

$$I_s = \frac{I_1}{\exp\left(V_1/nVt\right)} \qquad (4.6)$$

Table 4.3 summarizes the estimated values for *n* and its corresponding saturation current for each slope.

Table 4.3: *Estimated ideality factor and saturation current from I-V curves of M-PiN and M-MCPD rectifiers.*

Device	$\tau_{n,p}$	n_1	Is_1	n_2	Is_2
M-PiN	50ns	1.24	1.64×10^{-9}	2.0	7.32×10^{-7}
	1μs			1.53	1.44×10^{-9}
M-MCPD	50ns	1.3	2.56×10^{-9}	2.0	8.87×10^{-7}
	1μs			1.26	1.81×10^{-10}

Equation (4.2) shows that increasing τ_a (or the diffusion length L_a) results in an increase in the injected carrier concentration in the base. This has the well-known effect of enhancing the conductivity modulation, thereby reducing the base voltage V_m. In those diodes in which a single slope is presented, and is also near 2, it could assume that this regime dominates [36]. However, as discussed in section 1.3.3, there is an optimum value of L_a (and hence τ_a), beyond which any further increase in L_a actually causes an increase in the forward drop.

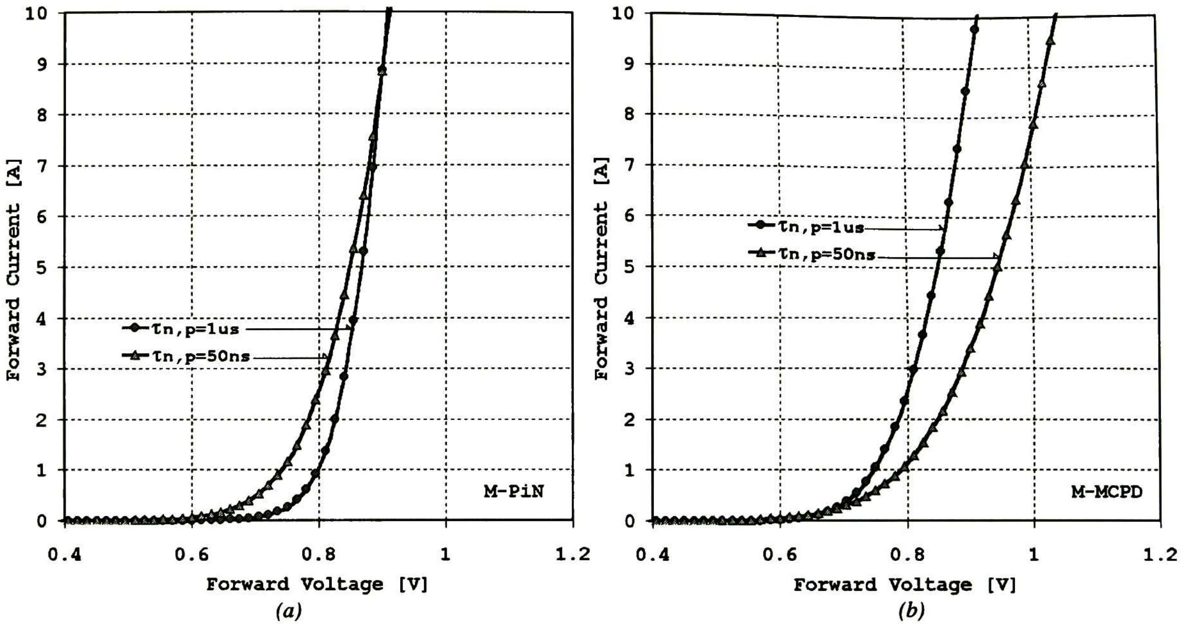


Figure 4.9: *I-V Characteristics as a function of the carriers lifetime. (a)M-PiN; (b) M-MCPD.*

In eq. (4.3) J_{nP+sat} is the 'saturation current'; D_{nP+}, L_{nP+}, d_p, N_A^-, and n_{p0} are the electron diffusion coefficient, electron diffusion length, the P^+ region length, and the P^+ region doping and electron concentration in the P^+ region, respectively. n_{iP+}^2 is the intrinsic carrier concentration in the P^+ region. It can be seen from the above two equations, for a given base width, the smaller the lifetime, the larger is the current. *Figure* 4.9 shows the lifetime effect in both rectifiers, M-PiN and M-MCPD. The diode current was computed for different values of carrier lifetime for the two structures, 50ns and 1μs.

When the M-PiN diode is forward-biased well below ≈0.9V, the computed current is higher for the shorter carrier lifetime. This indicates that the current is recombination dominated, which is also confirmed by the ideality factor of 2. The current in logarithmic scale versus voltage in linear scale for both rectifiers is shown in *figure* 4.10. From this *I-V* plot, the simulated characteristics using the shorter carrier lifetime, clearly shows the three different dependencies: for low injection levels a standard V/Vt characteristic is found. As the injection increases the dependence bends to a $V/2Vt$. Finally, beyond the voltage V_F(max), the diode operates under high-level injection. Here the resistance of the neutral N and P-type regions produce ohmic voltage drops which tends to reduce the current increase. As these drops becomes more dominant, the diode current stops increasing exponentially and becomes more proportional to the bias voltage.

Simulated characteristics using carrier lifetime of 1μs present only two regions of operation. Superimposed on these plots are straight lines representing the regions where the current varies as $\exp(V/nVt)$ with n designed as the *ideality factor*. Estimated parameters, the ideality factor n and saturation current Is, can be found as follows. Select two data points, I_1-V_1 and I_2-V_2, from the same straight line. Using the values of current and voltage corresponding to these points in the diode equation:

$$I \cong I_s \exp(V / nVt), \tag{4.4}$$

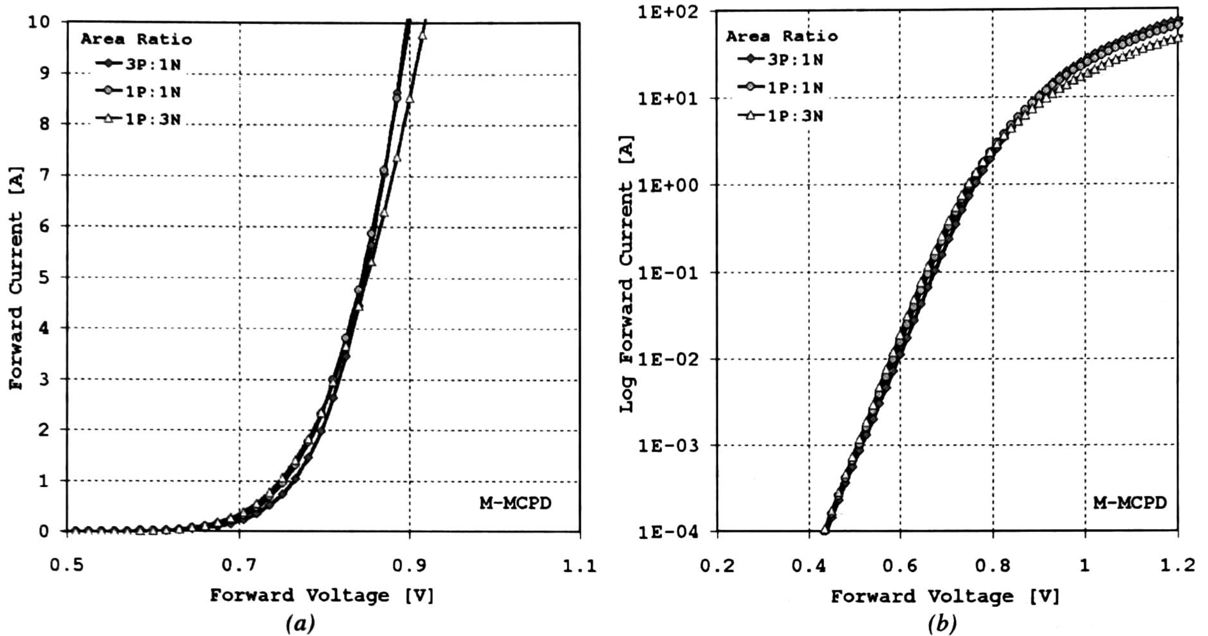


Figure 4.8: *Comparison of the on-state characteristics, for the three mosaic area ratios variants of the M-MCPD, $\tau_{n,p}=1\mu s$. (a)Lineal scale; (b)semi-log scale.*

The forward *I-V* curves of the studied M-MCPD with the three design variants are shown in *figures* 4.8. The differences between the curves are very small. It is shown that the forward voltage drop is not quite affected by the area ratio. Only towards currents of 10A, the area ratio starts to have an influence upon the on-state voltage. For the nominal load current, at 8A, the 1P:3N ratio with $V_F \approx 0.893V$ presents the worst case. Nevertheless, this result shows a good agreement with the specification data. For smaller current levels, e.g. at 3A, the curves practically lie on top of each other. Since the aim of the analysis is on estimating the forward voltage drop of the M-MCPD compared with the conventional one, from now on, the 1P:3N mosaic area ratio was selected to be compared with its conventional counterpart, the non-mosaic contact. For high forward voltage the lifetime does play only a minor role. In fact an increase of the lifetime implies an increase of the recombination and then, in the field driven regime, a reduction of the total current [27]. But the lifetime, in the regime in which the transport mechanism is diffusive (low and medium forward voltage) has a major impact [33]. Indeed by decreasing the lifetime the recombination current in the base should be increased, as pointed out by equation (1.23) which is rewritten here:

$$J = J_m = \int_{-d}^{+d} qUdx = \frac{q}{\tau_a}\int_{-d}^{+d} n(x)dx = \frac{2q\bar{n}d}{\tau_a} \tag{4.2}$$

here, τ_a is the ambipolar lifetime in the drift-region, $\bar{n}$ is the average injected electron/hole concentration in the drift-region, $d=W/2$ where W is the base width. At the end regions the increase of the current is proportional to (see eq. (1.30) in section 1.3.3)

$$J_{nP+sat} = q\frac{D_{nP+}}{L_{nP+}}\coth\left(\frac{d_p}{L_{nP+}}\right)\cdot n_{p0} = q\frac{\sqrt{Vt\cdot\mu_{nP+}}}{\sqrt{\tau_{nP+}}}\coth\left(\frac{d_p}{L_{nP+}}\right)\cdot\frac{n_{iP+}^2}{N_A^-} \propto \frac{1}{\sqrt{\tau_{nP+}}} \tag{4.3}$$

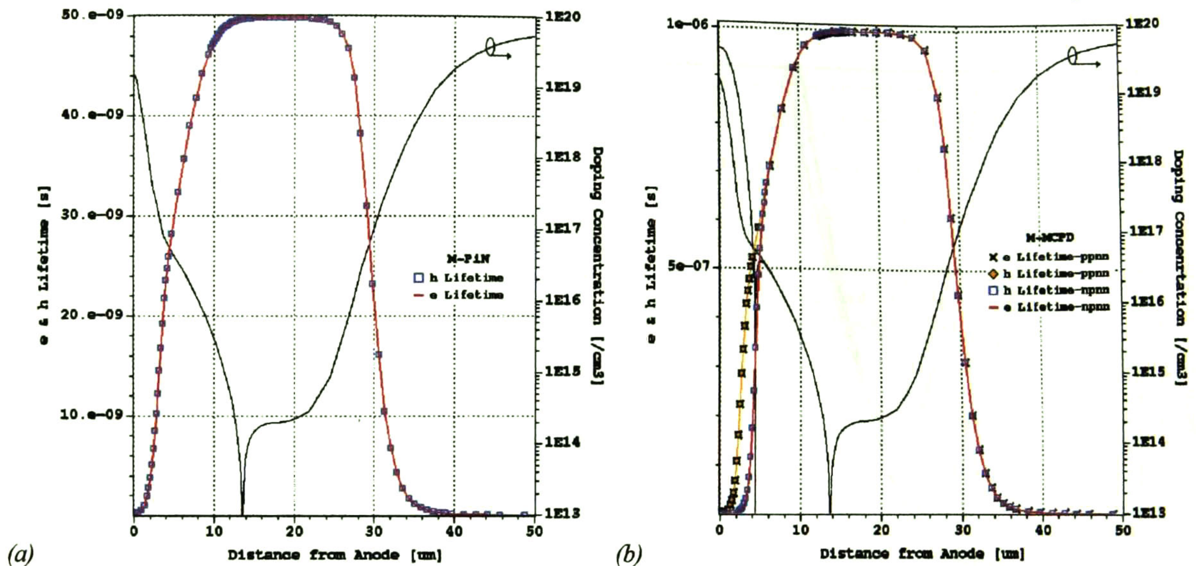


Figure 4.6: *Lifetime profiles computed from eq. (4.1). (a)M-PiN; (b)M-MCPD.*

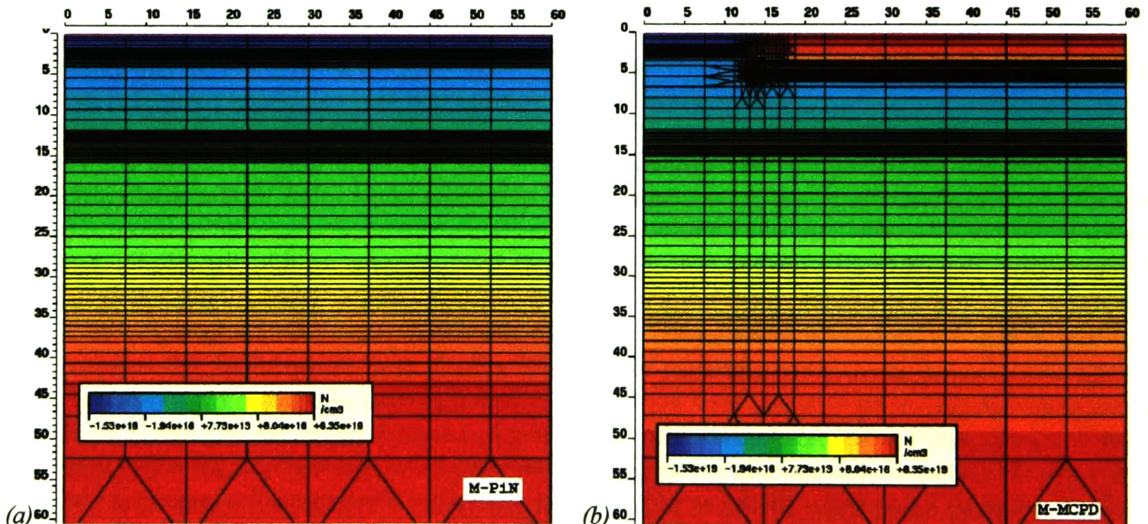


Figure 4.7: *2-D Device boundary and mesh generated in* MDRAW-$_{ISE}$ *for device simulation in* DESSIS-$_{ISE}$. *(a)M-PiN; (b)M-MCPD_1P:3N.*

4.4. Forward Properties

After the technological simulation provided satisfactorily results for creating power devices, a generation of a suitable grid using MDRAW-$_{ISE}$ was done. *Figure* 4.7 shows the 2-D finite element mesh results adequate for electrical device simulation to obtain as good information as possible about the key effects located very near the junctions. The regions of the substrate remains with a coarse mesh. This mesh refinement decreases the number of nodes and improves the execution time. Power devices were electrical simulated using DESSIS-$_{ISE}$. At this stage of the simulation, the devices can be simulated with their real dimensions. Since in 2-D, the device is assumed to be 1μm area factor depth, the contact area is calculated by multiplying the length of the contact by `1xAreaFactor`[μm]. In order to get a device area of 0.030cm^2 (≈3x10^{6}μm^2) with a contact length of 60μm, the "`AreaFactor`" used is 50,0132.

4.3. Lifetime Assessment

The lifetime is the average time between generation and recombination of a carrier. Low-level injection lifetime is generally given as one majority and one minority carrier lifetime. In high-level injection, where the carrier densities are more or less identical, electron and hole lifetimes need to be identical as well. This gives rise to high-level injection lifetime, the *ambipolar* lifetime, which is the same for both carrier polarities. The carrier lifetime reflects in the carrier distribution, and is an important parameter for the device performance.

Doping dependence has been implemented according to empirical formulas such as Scharfetter's relation [73]; see eq. (4.1), as well as temperature dependence based on equal empirical observation (see Chapter 3).

$$\tau_{n,p} = \tau_{min_n,p} + \frac{\tau_{max_n,p} - \tau_{min_n,p}}{1+\left(N/N_{ref}\right)^{\gamma}} \quad \text{where} \quad \begin{array}{l} N\text{=Net doping concentration,} \\ \tau_{n,p}=\tau_0 \text{ electron and hole lifetimes,} \\ N_{ref}=const. =7\text{x}10^{16}\text{cm}^{-3}. \end{array} \tag{4.1}$$

Since lifetime engineering has become an integral part of power device manufacturing, it is necessary to include lifetime control into device simulation. Lifetime control introduces many new parameters for device simulation. Implementing the trap profiles in device simulation is not a trivial task. Many factors are involved in determining the nature of the traps, such as the annealing process and the starting substrate material. Further investigation is necessary to demonstrate the actual position of the recombination trap levels and their effects on high-level lifetime.

Consequently, the effect of lifetime control is rendered by changing the carrier lifetime, $\tau_{n,p}$. Electron and hole lifetimes in the drift-region of the M-PiN structure of τ_n=50ns and τ_p=50ns were used as determined from measured data reported in [85]. However, this lifetime value along with the default recombination model parameters cannot accurately predict both static and transient characteristics unless the recombination trap energy level *Et* for Platinum used as a diffusing specie is set to 0.42eV above the valence band [7]. That means, lifetime model parameter "Etrap" in the device simulator **DESSIS**$_{\text{ISE}}$ (see Chapter 3) is changed from 0eV (default) to –0.14eV (*Etrap=Et-Ei*=0.42eV-0.56eV).

In the case of the M-MCPD, where no lifetime control is assumed, the τ_n and τ_p values are in the order of 1µs to describe drift-region. The default recombination model parameters was used, that means, the worst case for SRH recombination mechanism. In an earlier work [86], a comparison between these two structures with no lifetime control ($\tau_{n,p}$=5µs in both structures) was presented to demonstrate the feasibility of the mosaic contact concept.

Figure 4.6 shows the lifetime profiles for each structure under study. The doping profile is also shown as a reference. As it can be seen, the curves of electron and hole lifetimes lie on top of each other. The differences between the lifetime's values in the M-MCPD structure are due to the difference between P^+ and N^+ region doping concentration which form the anode mosaic contact. Notice the uniform carrier lifetime in the drift-region for both structures.

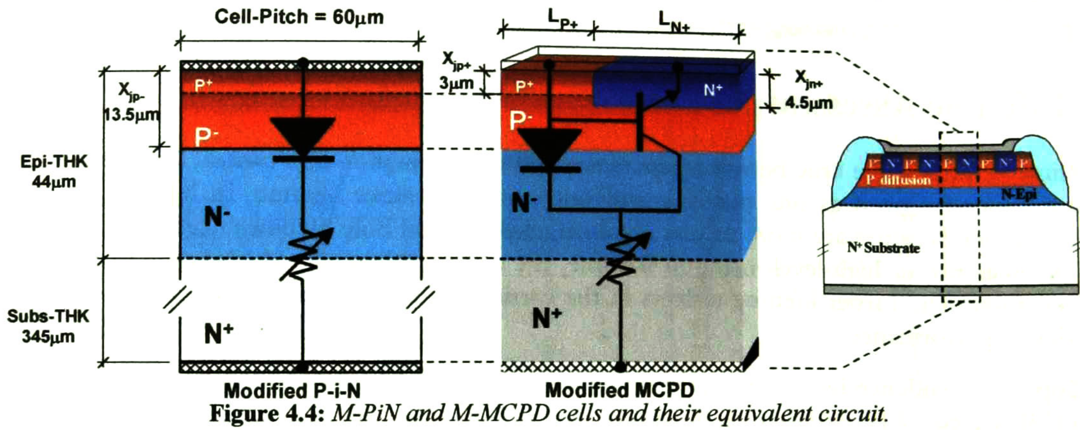


Figure 4.4: *M-PiN and M-MCPD cells and their equivalent circuit.*

Figure 4.5: *Final mesh and doping profile of the M-PiN and the M-MCPD. 2-D in (a) and (b); 1-D in (c) and (d). Plots were taken along a cut line in the middle of each section, A-A' ppnn-section and B-B' npnn-section.*

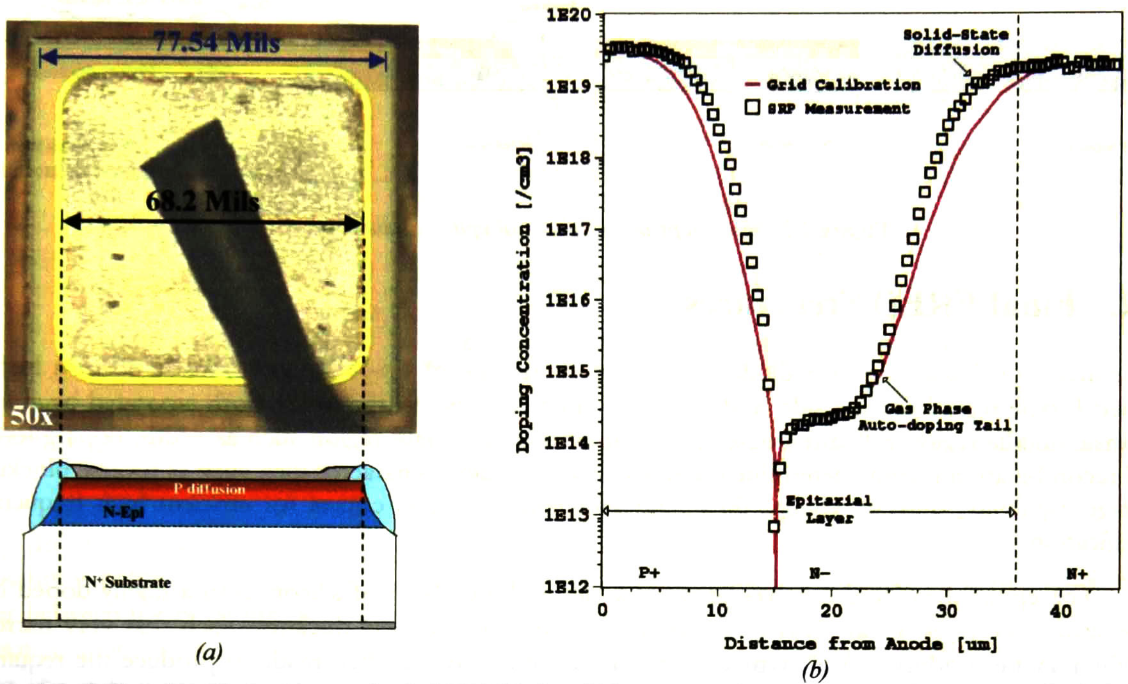


Figure 4.3: *(a)Top view photomicrograph of a* MUR820 *die. (b)Comparison between an actual SRP and 1-D simulated doping profile.*

Three different mosaic area ratios were studied: a)L_{P+}=45μm, L_{N+}=15μm (3P:1N); b)L_{P+}=30μm, L_{N+}=30μm (1P:1N) and c)L_{P+}=15μm, L_{N+}=45μm (1P:3N). Therefore, long strip patterns of each mosaic region form the anode contact. Here L_{P+} and L_{N+} are the P^+ and N^+ region lengths of the mosaic contact, respectively. The unit cell and the equivalent circuit of the M-MCPD and the Modified P-i-N (M-PiN) structures are shown in *figure* 4.4. *Figure* 4.5 shows the 2-D grid and the 1-D doping profile of the devices under study. The plots were taken along a cut line in the middle of each section, line A-A' *ppnn*-section and line B-B' *npnn*-section. Table 4.2. summarizes the final parameters for each structure after the technological simulations were performed.

Appendix B includes the simulation input command files used to generate the ISE-TCAD simulation in $DIOS_{-ISE}$ program of the structures mentioned above, so that for future research these results could be reproduced.

Table 4.2: *Final parameters of the structures under study.*

Structure	Anode	[a]N_B [cm^{-3}]	Epi-THK [μm]	[b]Cs [cm^{-3}]	[c]Xjn [μm]	[d]Xjp [μm]	Subs-THK [μm]	Rho-Subs [Ω-cm]	Area [cm^2]
Modified P-i-N	p-	2x10^{14}	44	1.0x10^{17}	-	13.5	345	0.00145	0.030
	p+			1.5x10^{19}		3.0			
Modified MCPD	p-			1.0x10^{17}	-	13.5			
	p+			1.5x10^{19}		3.0			
	n+			4.5x10^{19}	4.5				

[a]N_B = Base concentration or drift-region concentration (epi-layer).
[b]C_S = Surface concentration in a Gaussian diffusion profile.
[c]Xjp = Boron junction depth in the anode.
[d]Xjn = Phosphorus junction depth in the anode.

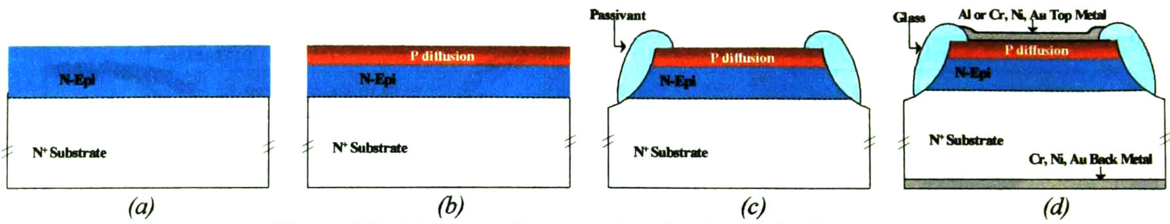


Figure 4.2: *Main steps in conventional epitaxial diode process.*

4.2. Final FRED Structures

All conventional silicon power diodes consist of some type of P-i-N structure, made up of a highly doped P-type region on one side, and a highly doped N^+ type on the other, both separated by a near intrinsic middle region called the base. The properties of this base region such as width, doping levels and recombination lifetime determine the most important diode characteristics, such as reverse blocking voltage capability, on-state voltage drop, and switching speed, all critical for efficient high frequency rectification.

The epitaxial method involves growing a lightly doped layer of silicon onto a highly doped N^+ type wafer; see *figure* 4.2(a). This gives accurate control of the base thickness such that very narrow widths may be produced. A P^+ type diffusion into the epi layer is then made to produce the required P-i-N structure; see *figure* 4.2(b). To ensure that the maximum reverse blocking potential of the diode is achieved, it is necessary to ensure that high fields do not occur around the edges of the chip. This is achieved by etching a trough in the epitaxial layer and depositing a special glass into it; see *figure* 4.2(c). Known as full mesa glass passivation, it achieves stable reverse blocking characteristics at high voltages by reducing charge build-up, and produces a strong chip edge, reducing the risk of assembly damage. This means that the diodes are rugged and reliable, and also allows all devices to be fully tested on-slice. Finally, *figure* 4.2(d) shows the diode after it has been metalized. The rectifier is then assembled into a wide selection of different power packages, the standard TO-220 outline being one example.

Figure 4.3(a) shows the photomicrograph of a MUR820 die. The effective conduction area of the die is 68.2Mils x 68.2Mils. Grid refinement criteria, according to the automatic grid adaptation, for technological process simulations of power diode structures was chosen to match an actual measured spreading resistance profile (SRP) from this commercial power rectifier. In spite of the theoretical unlimited number of grid points on which the device simulator $DIOS_{-ISE}$ can work, the number of mesh vertices was limited to the reasonable value of 50,000 for 2-D simulation. *Figure* 4.3(b) shows the comparison between the SRP and the 1-D simulated doping profile. Notice that auto-doping epitaxial layer effects were taking into account as a function of P^+ emitter diffusion conditions.

Therefore, based on conventional process parameters and device structure geometry information, a detailed numerical analysis of the proposed power rectifier diode was carried out. Simulations were done with a starting material <111> oriented N-type silicon substrate of 0.00145Ω-cm ($\approx 6.35 \times 10^{19} cm^{-3}$) resistivity and 345μm thickness. The high-low N^+-N^- junction was made by the subsequent epitaxial deposition of 20Ω-cm ($2 \times 10^{14} cm^{-3}$) 44μm thickness phosphorus doped N-type into the substrate. Thus, the die thickness was 15.3Mils. The P^+/N^+ mosaic contact is formed on the anode's surface by selective phosphorus and boron diffusion through its corresponding oxide mask. The effective cross section area is $0.030 cm^2$, but to reduce net points, the total cell width of the simulated structures was 60μm (same as the mosaic pitch), which was kept constant.

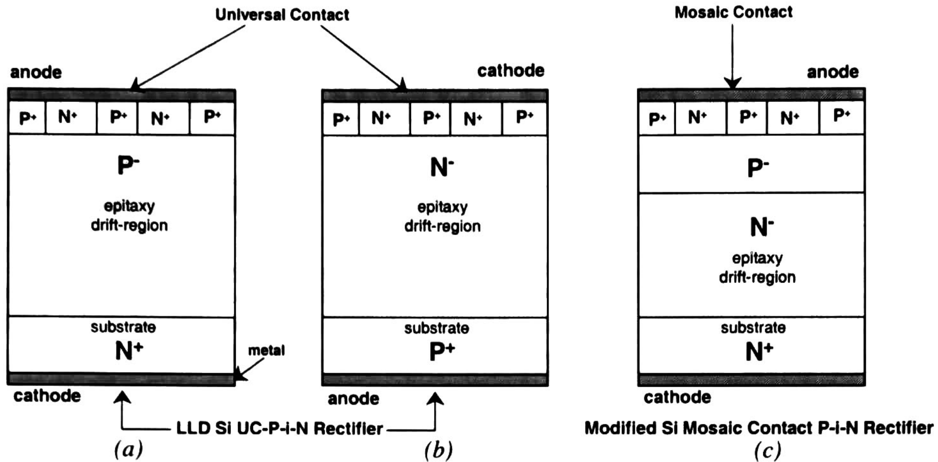


Figure 4.1: *(a) and (b) Cross-sectional view of Low-Loss High-Speed rectifiers with universal contact, and (c)Modified Mosaic Contact P-i-N Diode.*

In this thesis, a punch-through Modified Mosaic Contact P-i-N Diode (M-MCPD) rectifier structure is proposed; see *figure* 4.1(c). The modified MCPD consists of a lightly doped N-type epitaxial layer between the N^+ substrate (conventional epitaxial process) and a diffused P-region where the anode mosaic contact is placed. Proper adjustment of impurity concentration in the P^- region and the N-type layer makes it possible to increase the blocking voltage without sacrificing the forward voltage drop. This M-MCPD would be suitable for monolithic combination with a power transistor because this is made by a conventional double diffusion process used for most commercial transistors. In all these structures the anode is engineered to reduce the injection efficiency and thus obtain the lower stored charge that is required to achieve faster switching.

In further sections, comparisons between the M-MCPD and non-mosaic contact cases will be made. The effectiveness of the technique at improving speed and forward voltage drop will also be discussed. M-MCPDs were performed as possible consistent with the current static and dynamic specifications showed in Table 4.1.

Table 4.1: *Device Specifications.*

Blocking Voltage at Reverse Current $V_R@I_R$	Forward Voltage at Forward Current $V_F@I_F$	Max. Reverse Recovery Time t_{rr}
V_R=200V@5μA	V_F=0.975V@8A	35ns

These devices are intended for use as free wheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. The aim of investigating M-MCPDs is to determine the possibility of eliminating the platinum doping process used to reduce the reverse recovery time and stored charge in commercial devices.

Two-dimensional drift-diffusion numerical simulations (technological, electrical and mixed-mode) presented in this chapter are aimed to compare the devices from the fairest perspective possible. Unless otherwise specified, the static and dynamic analysis were carried out operating at T=300K. Self-heating effects were not taken into account. Simulation results are compared to experimental results to verify the benefits that a proposed structure provides compared with a commercial one (MUR820). Hence justify their industrial level production.

Chapter 4

Numerical Simulation Results and Analysis

Here, the theory presented in previous chapters will be numerically performed through the investigation of the main electrical parameters of power rectifier diodes. Technological, electrical and mixed-mode simulations are carried out using ISE-TCAD (2-D device, circuit and system simulator) based on standard process and device information of a commercial power rectifier. Finally, simulation results are compared to experimental results of a real device.

4.1. Introduction

Since the introduction of modern fast power switches, such as the IGBT, diodes in many applications are subjected to high voltage and current levels, and are required to switch at much higher speeds and frequencies. The most significant demands on fast power rectifier diodes are:

- High breakdown voltage.
- Low leakage current.
- Low forward voltage drop.
- Short reverse recovery time.
- Low reverse recovery charge.
- Low forward recovery voltage.
- A suitable shape for reverse recovery current (soft recovery).

Manufacturers designs are to meet these requirements. In spite of significant progress in the development of power diodes, no diodes are available that simultaneously have all of these properties. A high blocking voltage requires a wide lightly doped base, whereas a low forward voltage V_F needs a narrow base. Using a short base recombination lifetime produces faster recovery times, but this also increases V_F. Furthermore, in any P-N junction rectifier operating at high currents, carrier injection into the base takes place from both the P^+ and N^+ regions, helping to maintain a low V_F. There is always a trade-off between the on-state losses and breakdown voltages, and trade-off between the on-state losses and switching speeds. The requirements of the specific application must be matched to the capabilities of the available suitable diodes. This often requires certain device design approaches.

One promising approach to achieve a better trade-off between forward drop and switching speed of Fast Recovery Epitaxial Diodes (FREDs) is the Low-Loss and High-Speed Diode (LLD) structure containing an "universal contact" (UC) with a mosaic of P^+ and N^+ regions [1]. Since no lifetime control was necessary, e.g., Gold doping, a considerable improvement in the leakage current can be also observed.

To create the ideal ohmic contact with an epitaxial process, the conventional process (with an N-type epitaxial layer grown on an N^+ substrate) must be altered to a P-type epitaxial layer grown on an N^+ substrate (or an N-type epitaxial layer grown on a P^+ substrate); see *figure* 4.1(a) and (b). This makes the surface of the epitaxial layer accessible to subsequent diffusion of the P^+ and N^+ regions to form the UC. The reverse blocking voltage of an LLD is limited either by avalanche breakdown of the N^+-P^- (or P^+-N^-) junction or by punch-through of a depletion layer spreading from the N^+ substrate toward UC. Decreasing in doping concentration in the P^- region increases the breakdown voltage, but lowers the punch-through voltage, so that a trade-off is needed.

Simulation guided design method is able to accelerate the development of a semiconductor device by reducing the time for an improvement step significantly which ultimately results in lower costs. The simulation of power semiconductor devices is faced with several problems that are not found in VLSI device modeling, due to the huge and often complicated structures, the interaction with the external circuit environment, etc.

After having calibrated the simulators it is possible to get important device parameters immediately after a design change. Without calibration the TCAD tools may give unsuitable trends of the targeted value when a parameter is varied. The goals of process and device modeling can be summarized as follows:

1) simulate process runs;
2) gain an understanding of the process and device behavior;
3) process optimization;
4) perform controlled "experiments" (easy variation of design parameters);
5) perform "experiments" that otherwise would be impossible;
6) fast return of results because device variations do not need to be manufactured;
7) make use of device internal parameters which are otherwise inaccessible to direct measurement (e.g. current-densities, the electric field, or temperature-distributions);
8) analyze very fast phenomenon, like switching behavior, without the influence of unwanted parasitic elements in the setup.

Finally, in the present chapter the main physical model implemented in the numerical simulator have been reviewed beside a detailed description of the programs included within the ISE-TCAD simulation software package.

allowing the diode to reach its stable conduction state. I_F is adjusted by resistor *R*. The forward commuting di_F/dt is dependent on the applied forward voltage V_F. and the forward biasing circuit inductance *L*. Where $di_F/dt = V_F/L$. The circuit must allow the reverse voltage V_R to appear across the DUT at the end of the reverse recovery period. At this point the full blocking state is established across the diode *pn* junction.

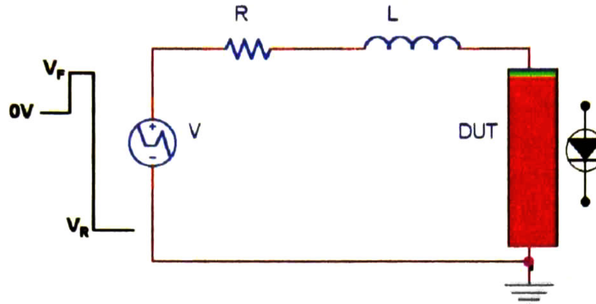


Figure 3.9: *Schematic of the reverse recovery circuit used for mixed-mode simulation of P-i-N diode.*

Current and voltage waveforms of the transient simulation are shown in *figure* 3.10

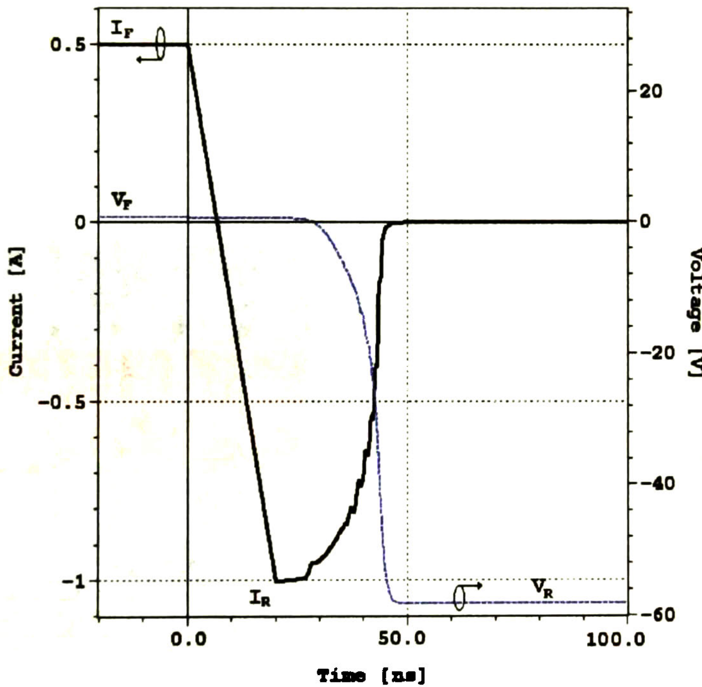


Figure 3.10: *P-i-N diode voltage and current waveforms during the switching mode operation.*

3.6. Summary

Through the years, several computer programs have been introduced to solve systems of partial differential equations which arise from problems in applied physics. Therefore, use of this tools requires very good physical background knowledge. As a result, the TCAD simulation has become a standard tool in electronics, since at the present time semiconductor devices cannot be manufactured without being simulated to predict the possible behavior that they will have in the reality.

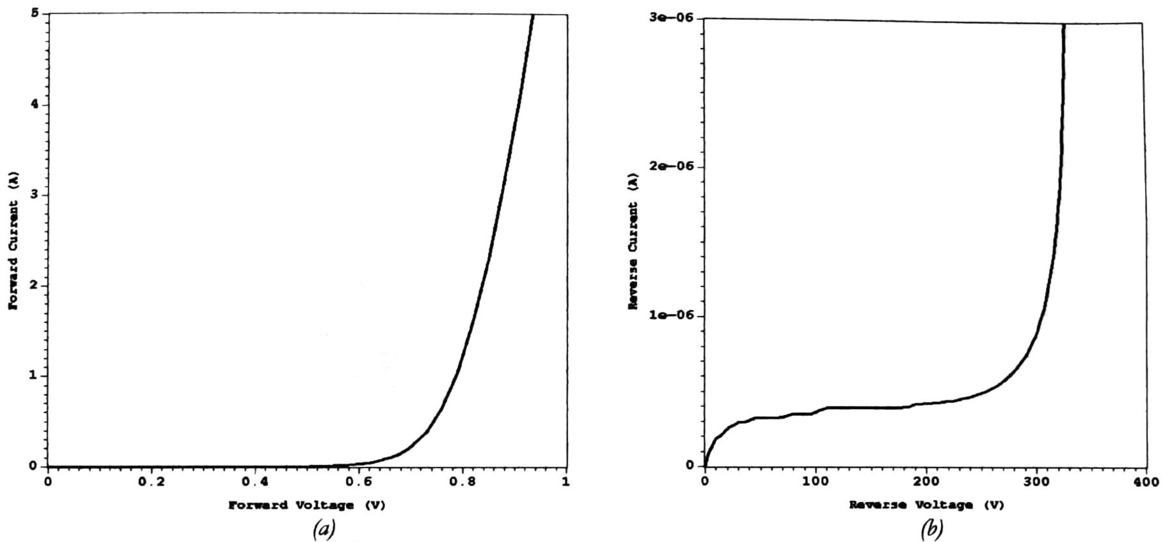


Figure 3.7: *(a)Forward and (b)Reverse I-V static characteristics of a P-i-N diode (INSPECT).*

Figure 3.8 shows the electric field behavior in 1-D and 2-D represented as vector arrows pointed to show the flow of the electric field. These results were obtained combining PICASSO$_{-ISE}$ and INSPECT$_{-ISE}$.

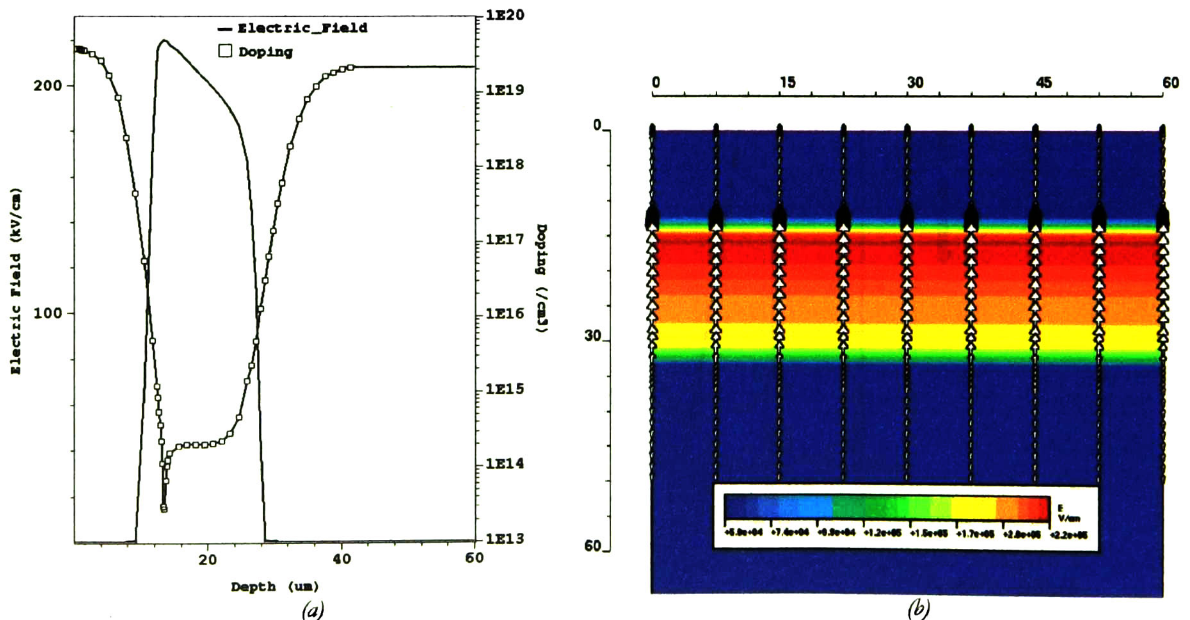


Figure 3.8: *P-i-N diode: (a)1-D electric filed and doping profile* (INSPECT); *(b)2-D electric field* (PICASSO).

Example 3.2: ***Transient Simulation.*** As an example of the mixed-mode simulation environment, the performance of the 2-D P-i-N diode in their switching application is simulated. All transient simulations are carried out by creating the input file **transient_des.cmd** (see Appendix B.3.). For the sake of numerical convergence, the circuit used in the mixed-mode simulations is an ideal test circuit fixture showing in *figure* 3.9, but it retains the essential features of inductive switching behavior. The applied voltage is set by a time dependent voltage source through a piecewise linear function. The known forward current I_F through the **Device Under Test** (DUT), must flow for a sufficient period of time

G) Math Section: This section is used to specify error criteria and other mathematical criteria for the different solve commands. Two types of math entries exist: device-specific entries and global entries. Device-specific entries refer to parameters that affect the solve methods of a device. Global math parameters are not device dependent and affect the global solution methods.

Mixed Mode Simulation

Mixed-mode simulations were realized for different devices using device/circuit *Mixed-Mode* [12]. Mixed-Mode DESSIS$_{\text{-ISE}}$ [73] software tool provides the possibility of analyzing the behavior of devices electrically simulated in conjunction with other passive and active devices, voltage and current sources. A new section is introduced to the input file for this type of device/system simulations, which is referred to as the *System* section. A circuit netlist must be defined in the command file to connect the devices together in a similar way as is usually done in SPICE.

3.5.5. Visualization and Analysis of the Simulation Results

Once every simulation process has been developed, deploying the obtained results is a must, either in charts or in graphic form, in 1-D, 2-D or up to 3-D. This is necessary to discern between the prospective and not agreement specification results that are looking for in the design, and to compare new results with the simulations that have been run previously. Two programs are used for the visualization of the results, INSPECT$_{\text{-ISE}}$ and PICASSO$_{\text{-ISE}}$.

INSPECT$_{\text{-ISE}}$ [83] is a data display and analysis program. It works with curves specified at discrete points defined by an array of X coordinates and an array of Y coordinates called *datasets*. Usually, a dataset represents a physical quantity, such as voltage, current, time or distance.

PICASSO$_{\text{-ISE}}$ [84]—**P**ainting **I**nteractively **C**olored **A**nd **S**haded **S**imulation **O**bjects— is an interactive visualization tool with an object oriented user interface to visualize simulation results of semiconductor devices. Multi-dimensional finite element devices can be observed and manipulated with PICASSO$_{\text{-ISE}}$. The main features of this visualization tool are given below:

- Intuitive user interface.
- Command interpreter for batch job processing.
- Various rendering models: color interpolated faces, drawing of iso-lines, wave plots of 2-D devices, shaded iso-surfaces, etc.

The different drawing styles available with PICASSO$_{\text{-ISE}}$ allow to display the 2-D device mesh, doping distributions, electric field, etc. After the device has been displayed, a cut line could be drawn through the device and the data is then selected for viewing and for saving as a graph by using INSPECT$_{\text{-ISE}}$.

Example 3.1: *Steady-State Simulation.* In order to obtain the static *I-V* forward and reverse characteristics for 2-D P-i-N diode structure shown in *figure* 3.6, two input files need to be created: **forward_des.cmd** and **reverse_des.cmd** (see Appendix B.3). *Figure* 3.7 shows both the forward and reverse static characteristics for the given P-i-N diode. The diode had a forward voltage drop of 0.884 Volts at 3 Amps forward current. While the blocking voltage was 300 Volts at 0.9 μAmps.

$$G^{||} = \alpha_n n v_n + \alpha_p p v_p \tag{3.29}$$

where $\alpha_{n,p}$ is the ionization coefficient, and $v_{n,p}$ denotes the drift velocity. The ionization coefficients are expressed in function of the Chynoweth's law [81]:

$$\alpha(E) = \gamma a \cdot e^{-\frac{\gamma b}{E}} \tag{3.30}$$

with

$$\gamma = \frac{tanh(h\omega_{op}/2kT_0)}{tanh(h\omega_{op}/2kT)} \tag{3.31}$$

the factor γ with the optical phonon energy $h\omega_{op}$ expresses the temperature dependence of phonon gas against which the carriers are accelerated. The coefficients sued were measured by van Overstraeten and de Man [82]. For electrons: a=7.03x10^{5}cm^{-1}, b=1.231x10^{6}V/cm, and for holes: a=1.582x10^{6}cm^{-1}, b=2.036x10^{6}V/cm. The parallel electric field was chosen as a driving force.

***D) Plot Section*:** The *Plot* section is used to specify which data will be saved by the *Plot* command in the *File* section for visualization. Each data type is defined with a keyword and include a wide range of parameters such as *Potential, eDensity, hDensity, Doping, ElectricField, eLifeTime, hMobility, ConductionCurrent, SRHRecombination, etc.*

F) Solve Section: The *Solve* section is composed of a series of simulation commands to be performed which are activated one after another in the order of their appearance in the input file. Thus, the order of the solve commands and their hierarchy is important. The basic solution methods are:

(i) Coupled: activates a Newton like solver over a set of equation-variable pair, e.g., Poisson-electrostatic potential, electron continuity-electron density, hole continuity-hole density. The possible parameters of the command are the maximum number of iterations allowed, the desired precision of the solution, which linear solver should be used, and finally, whether the solution is allowed to become worse over a number of iterations.

(ii) Plugin: controls an iterative loop over two or more *Coupled* commands. It is used when a fully coupled method would use too many resources of a given machine or when the problem is not yet solved and a full coupling of the equations would diverge. It uses Gummel iteration which successively takes the solution of the variable from one equation and use it to solve the next equation in succession. Starting over with the first equation, and repeating until all the equations have converged to a solution.

(iii) Quasistationary: is used to ramp a device from one solution to another solution through the modification of its boundary conditions (e.g., ramping the voltage at a contact to perform steady-state simulations). The command must start with a device that has already been solved. The simulation then continues by iterating between the modification of the boundary conditions and re-solving the device.

(iv) Transient: performs a transient time simulation. The command must start with a device that has already been solved. The simulation then continues by iterating between incrementing time and re-solving the device.

with

$$n_1 = n_{i,eff} e^{\frac{E_{trap}}{kT}} \tag{3.22}$$

$$p_1 = n_{i,eff} e^{\frac{-E_{trap}}{kT}} \tag{3.23}$$

where E_{trap} is the difference between defect level and intrinsic level. E_{trap}=0 sets a single recombination level in the center of the bandgap. The minority carrier lifetimes τ_n and τ_p are modeled as a product of a doping dependent τ_{dop} and a temperature dependent $f(T)$ factor;

$$\tau_v = \tau_{dop} \times f(T), \quad v = n, p \tag{3.24}$$

The Scharfetter relation

$$\tau_{dop_n,p}(N) = \tau_{min_n,p} + \frac{\tau_{max_n,p} - \tau_{min_n,p}}{1 + \left(\frac{N}{N_{ref}}\right)^{\eta}} \tag{3.25}$$

is implemented as doping dependence of SRH lifetimes. $N_{ref_n,p}=7\times10^{16}cm^{-3}$ and $\eta=1$ are characteristic parameters dependent on both the material and the device technology. $\tau_{min_n,p}=0$ is set; the value of $\tau_{max_n,p}$ is customized on the parameter file *.**par** (see Appendix B.3.), e.g., $\tau_{max_n,p}=1\mu s$, 50ns. From measurements of the recombination lifetime $\tau=\delta n/R$ in power devices (δn is the excess carrier density under neutral conditions, $\delta n=\delta p$) it was concluded that the lifetime increases with rising temperature. Such a dependence was either modeled by a power law [78, 79]:

$$\tau(T) = \tau_0 \left(\frac{T}{300}\right)^{\alpha} \tag{3.26}$$

Auger recombination is modeled as follows:

$$C_n(n,T) = C_n(T)\left(1 + H_n e^{-\frac{n}{n0}}\right) \tag{3.27}$$

$$C_p(p,T) = C_p(T)\left(1 + H_p e^{-\frac{n}{p0}}\right) \tag{3.28}$$

where n_0 and p_0 are the densities at which excitons decay, and $C(T)(1 + H)$ are the low-injection Auger coefficients. Default values are $n_0=p_0=10^{18}cm^{-3}$, H_n=3.47, H_p=8.25. $C_n(n,T)$ and $C_p(p,T)$ represent the Auger recombination decrease at high carrier densities [80].

The model used to simulate avalanche breakdown ionization for the reverse-biased condition includes carrier generation due to impact ionization, with the generation rate G expressed as

$$\frac{1}{\mu_{low}} = \frac{1}{\mu_{dop}} + \frac{1}{\mu_{eh}} \tag{3.17}$$

where μ_{dop} is the doping dependence mobility expressed as [75]:

$$\mu_{dop} = \mu_{min1} \exp\left(-\frac{P_c}{N}\right) + \frac{\mu_{cont} - \mu_{min2}}{1+\left(\frac{N}{C_r}\right)^{\alpha}} - \frac{\mu_1}{1+\left(\frac{C_s}{N}\right)^{\beta}} \tag{3.18}$$

here, N is the total doping concentration, the bulk mobility μ_{const} is a temperature dependent constant [76]:

$$\mu_{const} = \mu_L \left(\frac{T}{300}\right)^{\zeta} \tag{3.19}$$

the subscript L refers to "lattice". All parameters are collected in Table 3.1.

Table 3.1: *Constants used for Bulk Mobility Calculations in eq. (3.19)*

Constant	Phosphorus	Boron	Unit
μ_{min1}	68.5	44.9	cm^2/Vs
μ_{min2}	68.5	0	cm^2/Vs
μ_L	1414	470.5	cm^2/Vs
ζ	2.2	2.5	--
μ_1	56.1	29.0	cm^2/Vs
C_r	9.20×10^{16}	2.23×10^{17}	cm^{-3}
C_s	3.41×10^{20}	6.10×10^{20}	cm^{-3}
α	0.711	0.719	--
β	1.98	2.0	--
P_c	0	9.23×10^{16}	cm^{-3}

Carrier-carrier scattering (electron-hole scattering "eh") μ_{eh} is included to account for ambipolar transport effects [77]:

$$\mu_{eh} = \frac{D\left(\frac{T}{T_0}\right)^{3/2}}{\sqrt{np}} \left[ln\left(1 + F\left(\frac{T}{T_0}\right)^2 (pn)^{-1/3}\right)\right]^{-1} \tag{3.20}$$

the coefficient values are D=1.04x10^{21}(cmVs)$^{-1}$ and F=7.452x10^{13}cm$^{2/3}$.

(iii) Generation-Recombination.- Recombination mechanisms include the Shockley-Read-Hall (SRH) recombination model stated as:

$$R^{SRH} = \frac{np - n_{i,eff}^2}{\tau_p(n+n_1) + \tau_n(p+p_1)} \tag{3.21}$$

$$n = \sqrt{\frac{(N_D - N_A)^2}{4} + n_{i,eff}^2} + \frac{N_D - N_A}{2} \tag{3.11}$$

$$p = \sqrt{\frac{(N_D - N_A)^2}{4} + n_{i,eff}^2} - \frac{N_D - N_A}{2} \tag{3.12}$$

For 2-D devices simulations, calculated currents are in units of A/μm. The *AreaFactor* specifies a multiplicative factor that multiplies the area of the electrode by a given amount. By default this value is set to 1 corresponding to 1μm depth of the device; the contact area is thus (length-of-contact x 1 x *AreaFactor*)μm^2. Setting the *AreaFactor* permits the adaptation of the operating currents for realistic device dimensions.

C) <u>Physics Section:</u> The *Physics* section is used to select which models will be used to simulate the device. These include:

(i) Temperature.- Specify the device lattice temperature in Kelvin. The default is 300K.

(ii) Mobility.- The mobility is modeled in a modular way. The high field mobility μ is given by a function of the low field mobility μ_{low} and of the driving force E:

$$\mu = f(\mu_{low}, E) \tag{3.13}$$

thus, the mobility model of high field velocity saturation is stated as [74]:

$$\mu(E) = \frac{\mu_{low}}{\left[1 + \left(\frac{\mu_{low} \cdot E}{v_{sat}}\right)^{\beta}\right]^{1/\beta}} \tag{3.14}$$

The component of the electrostatic filed takes the value of the gradient of the quasi-Fermi level, $E = |\nabla \varphi_{n,p}|$, the velocity saturation v_{sat} is defined as:

$$v_{sat} = v_{sat,0}\left(\frac{T}{T_0}\right)^{-v_{sat,exp}} \tag{3.15}$$

with $v_{sat,0}$=1.07x10^7cm/s, $v_{sat,exp}$=0.87 for electrons and $v_{sat,0}$=8.37x10^6cm/s, $v_{sat,exp}$=0.52 for holes. β is defined as:

$$\beta = \beta_0\left(\frac{T}{T_0}\right)^{\beta_{exp}} \tag{3.16}$$

with β_0=1.109, β_{exp}=0.66 for electrons and β_0=1.213, β_{exp}=0.17 for holes, μ_{low} depends on the following contributions:

$$\vec{J}_n = -nq\mu_n \nabla \phi_n \tag{3.6}$$

$$\vec{J}_p = -pq\mu_p \nabla \phi_p \tag{3.7}$$

here, μ_n and μ_p are the electron and hole mobility. The command DESSIS$_{-ISE}$ input file has the standard extension ***.cmd**; see Appendix B.3. This file is divided into sections. The sections that define the device are: *File, Electrode, Thermode, Interface, Physics,* and *Plot.* There are also sections to define the solve methods which are: *Math and Solve.*

A) File Section: In this section the file names for the simulations are specified. The main commands used to specify a device are,

Device input files:

Grid: Device geometry and mesh description file supplied by a mesh generator (**.grd**).

Doping: Device doping file describing impurity concentration, supplied by a mesh generator (**.dat**).

Load: Load and continue the simulation with old device results (**.sav**).

Parameters: Read and use model parameters from file for device (**.par**). A template parameter file is generated using the option `-P` for Si parameters. The templates, **dessis.par** is an ASCII file which can be renamed, modified and loaded in order to adjust parameters of the physical models (see Appendix B.3).

Device output files:

Save: At the end of the simulation, the solution is stored in this file for future use as the initial solution using the *Load* keyword. (**_des.sav**).

Plot: Store device plot output here for visualization with a graphics package (**_des.dat**).

Current: Store device currents, voltages, and temperatures for inspecting them with a graph tool (**_des.plt**).

Output: File for saving the global log file of the simulation. This file is a textual output description of the information created by the simulation (**_des.log**).

B) Electrode Section: Currents and voltages at the different device contacts are specified in this section. There must be at least one electrical contact defined for each device. Each contact is characterized by a contact name related to the definition in the mesh generation. The default electrical boundary conditions are ideal ohmic contacts. In this case, charge neutrality and equilibrium are assumed as:

$$n - p = N_D - N_A \tag{3.8}$$

$$np = n_{i,eff}^2 \tag{3.9}$$

For Boltzamann statistics this system of equations can be resolved:

$$\psi = V_{applied} + \frac{kT}{q} \operatorname{asinh}\left(\frac{N_D - N_A}{2n_{i,eff}} \right) \tag{3.10}$$

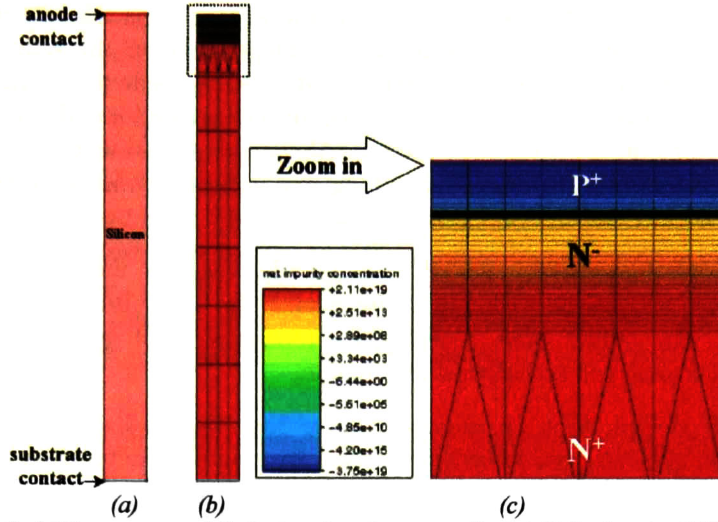


Figure 3.6: *(a)Geometry, and (b & c)mesh refinement of a P-i-N diode using* MDRAW$_{-ISE}$.

Drift-Diffusion Approach [73]

The three governing equations for charge transport in semiconductor devices are the Poisson's equation, solving for the electrostatic potential; electron current continuity equation, solving for the electron density n or electron quasi-Fermi potential; and hole current continuity equation, solving for the electron density n or electron quasi-Fermi potential. The Poisson's equation is stated as:

$$\nabla \cdot \varepsilon \nabla \psi = -q(p - n + N_{D^+} - N_{A^-}), \tag{3.1}$$

where ε is the electric permittivity, ψ is the electrostatic potential, q is the elementary electronic charge, n and p are the electron and hole densities, and N_{D+} and N_{A^-} are the number of ionized donors and acceptors, respectively. If the Bolztmann statistics is assumed, then:

$$n = n_{i,eff}\, exp(-q(\phi_n - \psi)/kT) \tag{3.2}$$

$$p = n_{i,eff}\, exp(-q(\phi_p - \psi)/kT) \tag{3.3}$$

where $n_{i,eff}$ is the effective intrinsic density, k is the Boltzmann's constant, T is the temperature, and ϕ_n and ϕ_p are the electron and hole quasi-Fermi potentials. The electron and hole continuity equations are written as follows:

$$\nabla \cdot \vec{J}_n = qR + q\frac{\partial n}{\partial t} \tag{3.4}$$

$$-\nabla \cdot \vec{J}_p = qR + q\frac{\partial p}{\partial t} \tag{3.5}$$

where R is the net electron-hole recombination rate and $\vec{J}_n$ and $\vec{J}_n$ are the electron and hole current densities, respectively, given as:

mesh refinement information by means of rectangular refinement areas. Usually the mesh density is adapted to the gradient of the impurity concentration. Depending on the refinement criterion, an element will be refined if the gradient or the difference of the data inside the element is greater than a certain value. This type of refinement is useful when the key effects are located very near the junctions, and the substrate region remains with a coarser mesh. Also, mesh refinement decreases the number of nodes and improves the execution time. The doping and refinement information is specified in a command file with extension ***.cmd** (See Appendix B.2).

Once the refinement conditions are set, building the mesh is the next task. The geometry description, doping and refinement information are read from files ***.bnd** and ***.cmd**, respectively. MDRAW$_{\text{-ISE}}$ creates the output files ***_mdr.grd**, containing grid geometry information, and ***_mdr.dat**, containing doping and refinement information.

The P-i-N diode design steps are shown in *figure* 3.6. *Figure* 3.6(a) represent the geometrical definition of the silicon substrate including the epitaxial layer and the defined contacts. The subMesh read from DIOS$_{\text{-ISE}}$ is the same as that shown in *figure* 3.5(a).

Figure 3.6(b) and (c) show the generated grid map of the device. It is quite clear that the initial mesh (subMesh) would have been ill-adapted to an accurate device simulation. Thus, the transition to the device simulation is carried out using the process technology simulation results in the mesh generator program, describing coarse and fine areas on the device structure to reduce net points and to optimize the device simulation.

3.5.4. Device and System Simulation

DESSIS$_{\text{-ISE}}$ [73] —**D**evice **S**imulation for **S**mart **I**ntegrated **S**ystems— is a multi-dimensional (1-D, 2-D and 3-D) device simulator with advanced physical models capable of predicting the electrical and thermal behavior of semiconductor devices and circuits. Its transport models range from simple drift-diffusion to electro-thermal and full six-equation hydrodynamics. DESSIS$_{\text{-ISE}}$ can perform stationary, transient and AC simulations. Multiple semiconductor devices and lumped elements (SPICE-like elements) can be combined in a single simulation, allowing complex, mixed device-circuit simulations.

In order to obtain "realistic results", it is mandatory to figure out which models should be used to proper represent the behavior of the structure under study. This is the reason why in the following paragraphs the main physical models implemented in the used simulator are reviewed. Depending on the device under investigation and the desired level of modeling accuracy, the user can choose between three simulation modes, conventionally named as:

Drift-Diffusion: Isothermal simulation, with stationary transport phenomenon (suited for low power density devices with long active regions).

Thermodynamic: Account for self-heating (suited for high power density devices with long active regions).

Hydrodynamic: Account for self-heating and non-stationary transport phenomenon (suited for devices with small active regions).

Both, static and dynamic numerical analysis were carried out using the Newton method by solving drift-diffusion models. In the following a brief description of the theoretical basis of this transport model is given.

domain. No closed-form solutions exist, and therefore only approximated solutions can be obtained. These solutions are computed by simulating a discrete representation of the PDEs over a spatial decomposition of the geometry of the device. Thus a *mesh* is required. A mesh is a spatial decomposition of a geometric domain into simple elements, usually triangles/tetrahedrons [71]. When computing approximate solutions, the transfer of qualitative properties from the PDEs to the discrete systems is critical. Major concerns are the stability of the solution and the accuracy together with an acceptable computing time and memory consumption. Therefore, the mesh has to be well adapted, e.g., its elements should be refined in regions where high errors in the solution and large gradients of important variables (doping, electric field, etc.) are expected. With a non-adapted mesh the recombination current at the junction cannot be calculated correctly. In conclusion, only with a problem specific adaptation of the grid a sufficiently accurate simulation is possible within reasonable calculation times.

MDRAW$_{-ISE}$ [72] is a program to create 2-D finite element (F.E.) meshes adequate for device simulation under the ISE-TCAD environment. In order to accomplish the grid generation task, MDRAW$_{-ISE}$ provides two major environments:

A boundary editor.
A doping editor.

Combining these two components it is possible to generate and modify meshes until they meet the specific simulation domain requirements.

1) *The Boundary editor:* The purpose of the boundary editor is to visualize and to modify any device structure. The main editing tasks that can be carried out are to simplify complex boundaries, to define contacts, and new layers, to specify the material in some layer, to merge different results, to delete parts of a device and to extract sub-devices. To begin with the editing of any device structure, two options are available:

1. Start from scratch and create a new device to get a fast prototype or to avoid the process simulation step.
2. Edit an existing device structure originated from a process simulator such as DIOS$_{-ISE}$ to simplify the geometry in order to avoid unnecessary points in the final device mesh (as in the case of this work).

The device geometry is stored in an input file with the extension ***.bnd**.

2) *The Doping editor:* The purpose of the doping editor is to visualize and to modify the doping description of the device. MDRAW$_{-ISE}$'s doping editor features include tools to create doping descriptions, to describe refinement conditions and finally to build a mesh meeting all the requirements needed for device simulation. Doping profiles can be defined in two ways:

1. Define an analytical doping profile which can be either a gaussian, an error function, a constant doping profiles, and lifetime profiles or an alpha particle profile. Additionally, a doping profile starting from a 1-D externally defined doping profile function can be defined.
2. Include external data from a process (DIOS$_{-ISE}$) or a device simulator (as in the case of this work).

The external data coming from DIOS$_{-ISE}$ is included as a reference mesh. Such a mesh is called a *subMesh* (see *figure* 3.5(a)). The mesh generator will interpolate data from the subMesh in order to perform *mesh refinement*. Once the doping profile information is included, the next step is to specify the

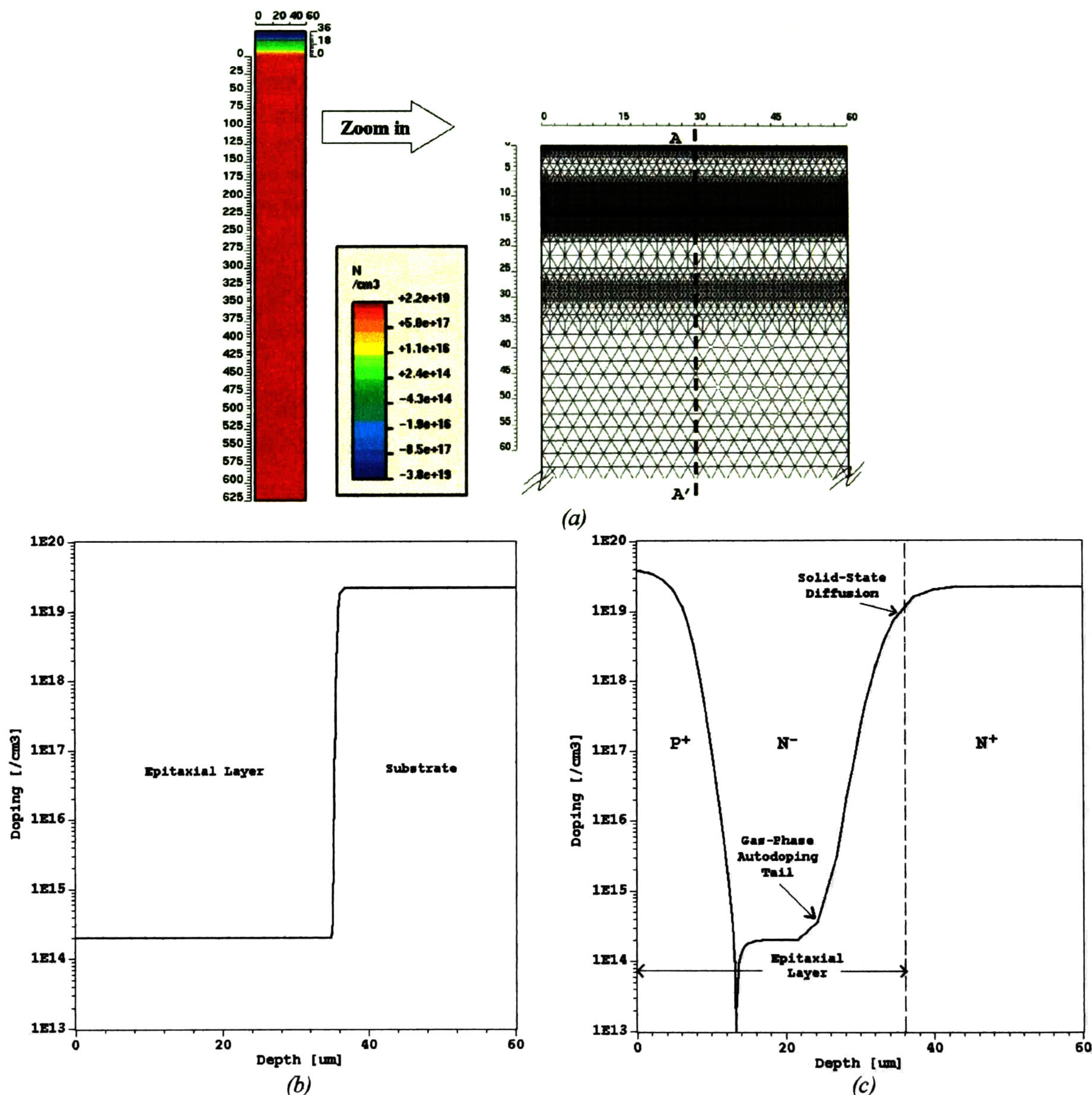


Figure 3.5: *(a)2-D automatic grid adaptation (final mesh); (b)1-D doping profile after epitaxial growth. (c)1-D final doping profile of a conventional P-i-N diode.*

In order to model the epitaxial growth and diffusion into silicon, the *Conventional* type diffusion model with the specific diffusion model of SUPREM-3 [70] selected for each of the dopants, e.g., boron and phosphorus, have been used. The diffusion model and parameters used for doping profile generation are presented in Appendix A.

3.5.3. Structure and Mesh Generation

As already mentioned above, the physics of semiconductor devices is described by tightly coupled non-linear PDEs. The semiconductor PDEs are difficult to solve due to the high degree of non-linearity involved. The PDEs must be solved with appropriate boundary and initial conditions over the device

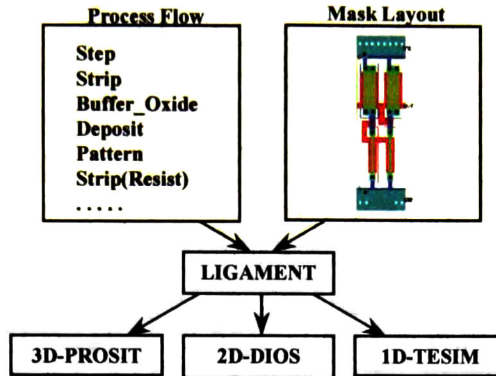


Figure 3.4: LIGAMENT$_{\text{-ISE}}$ *system overview.*

PROLYT$_{\text{-ISE}}$ [67] is the GENESISe$_{\text{-ISE}}$ layout editor. It can be used as an input editor for LIGAMENT$_{\text{-ISE}}$ to define 1-D, 2-D, and 3-D simulation regions, to add new polygons and rectangles to the original designer layout or remove existing ones, to change the position of layout elements, to set contacts for subsequent device simulation, and to parametrize the layouts.

3.5.2. Technological Process Simulation

The numerical process simulation program DIOS$_{\text{-ISE}}$ [68] —Diffusion Implantation Oxidation in Silicon— is a 2-D simulator which provides a user friendly input language to translate the process conditions into simulator input files. Local grid adaptation techniques are widely used in DIOS$_{\text{-ISE}}$ and to a large extent the adaptation is automated. Before starting a simulation run, the input files are checked for syntax errors. Integrated graphical facilities and interface programs to other simulation tools are supported. After each process' step an output of the layer system, doping profiles and the calculations of relevant device parameters (sheet resistance, junction depth, doping quality, threshold voltage, etc.) is possible. The following process steps can be simulated using DIOS$_{\text{-ISE}}$:

1. Ion implantation.
2. Diffusion, oxidation, predeposition, epitaxy, and silicidation.
3. Layer deposition and etching.

The process flow is entered in an input file with the extension ***.cmd**. The refinement criteria can be chosen to match an actual measured spreading resistance profile (SRP) according to the automatic grid adaptation, taking into account autodoping effect [69]. This effect results in an impurity redistribution during epitaxial growth and thermal processing by an impurity diffusion process from the substrate. *Figure* 3.5(b) and (c) show a 1-D doping profile after the epitaxial growth process and the final doping profile in the conventional P-i-N diode through the line A-A' showed in *figure* 3.5(a).

Dopant diffusion, chemical reactions at the interfaces and inside the layers and convective dopant transport by internal electrical fields, by material flow or moving material interfaces result in a dopant redistribution during all high temperature processes. The *Diffusion* command is used to simulate all high temperature steps (see Appendix B.1). The various process atmospheres are described by the parameter *Atmosphere=O2|HCl|H2O|H2O2|H2N2|N2|Epitaxy|Prebake|Mixture.*

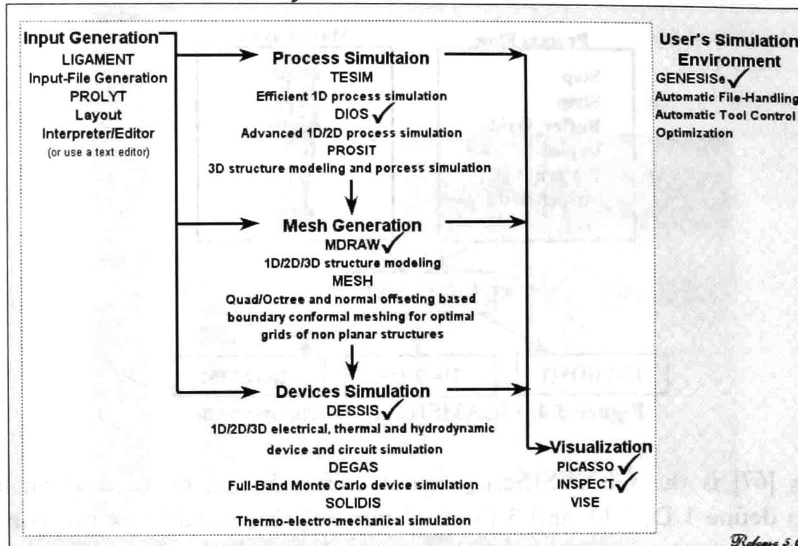


Figure 3.3: ISE-TCAD *Simulation System.*

The control and the feedback data path is provided by an extended work flow tool based on GENESISe$_{-ISE}$ [63] which is a graphic user interface (GUI). It aims at releasing the user from typing UNIX commands for data file handling or starting ISE applications.

Device and system simulation can be carried out from the early stages by defining the input-file generation and layout using LIGAMENT$_{-ISE}$ and PROLYT$_{-ISE}$, respectively, followed by the technology process stage using TESIM$_{-ISE}$ (1-D), DIOS$_{-ISE}$ (2-D) or PROSIT$_{-ISE}$ (3-D). The structure and mesh generation is then defined for the device using MDRAW$_{-ISE}$ or MESH$_{-ISE}$. Finally device and system simulations can be carried out using DESSIS$_{-ISE}$, DEGAS$_{-ISE}$ or SOLIDIS$_{-ISE}$ (see *figure* 3.3) to obtain the required results, which are then visualized and analyzed using programs such as PICASSO$_{-ISE}$ or INSPECT$_{-ISE}$. Since most of the work has been carried out starting from process simulation stage following by the marked programs on each stage in *figure* 3.3, only a brief description of the input-file generation and process layout are presented in the following section. A more detailed view of these programs is carried out in [64].

3.5.1. Input Generation and Layout Interpreter/Editor

LIGAMENT$_{-ISE}$ [65]] is a system designed for performing process simulations using an automatically generated process simulation input file. The information in this file includes technology characteristics and process parameters as well as information that governs behavior of graphics devices used by the design tools. The system is designed to work with a variety of different process simulators (e.g., 1-D, 2-D or 3-D). An overview of LIGAMENT$_{-ISE}$ is presented in *figure* 3.4. In order to generate process simulation input files, two main pieces of information are required. The first is a general description of the process flow given in the SPR (Simple Process Representation) language. The second is the layout for the device which is to be simulated. For layout files, LIGAMENT$_{-ISE}$ supports CIF (Caltech Intermediate Form) files [66].

In process simulation, one tries to simulate all fabrication steps of importance including implantation, diffusion, oxidation, etc., with the best possible physical model, usually at the level of PDEs that are solved numerically in one or multiple dimensions.

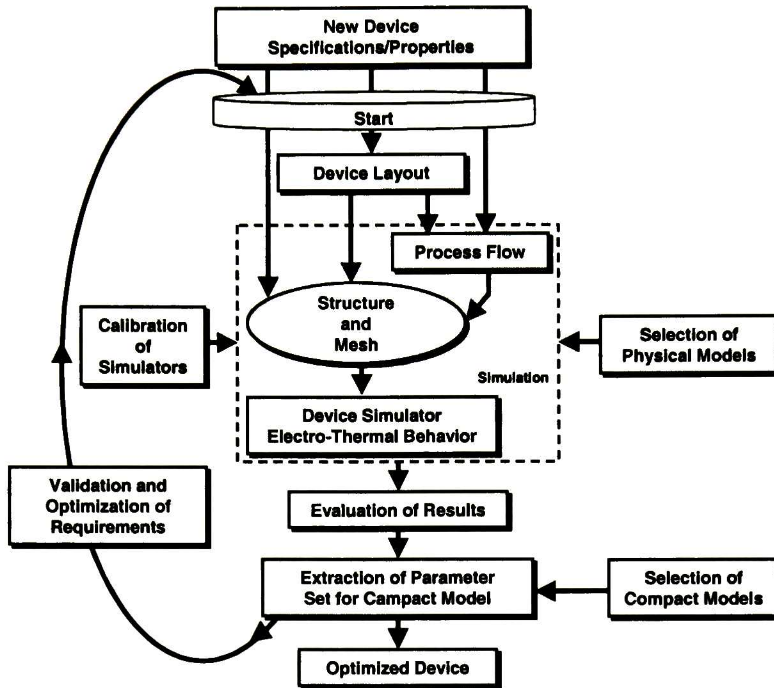


Figure 3.2: *Advanced TCAD design process [After Stricker et al.].*

Second group (Device/System) includes the design packages with complete simulation environments, better known as Virtual-Fab. These tools range from 1-D, 2-D and 3-D process simulators, sophisticated mesh generation and device editing programs to a complete device modeling environment that allows mixed-mode (device/circuit) electro-thermal analysis with multiple devices of arbitrary dimensions in a single problem. Between these programs stand out, SUPREM [58], PISCES [59], MEDICI [60], ATHENA and ATLAS [61], DIOS and DESSIS [62].

Some of the simulation programs mentioned above could be used for a given type of devices, while others have been designed for large number of structures. Advantages and disadvantages of each one of them depend on mathematical equation solutions, physical models, and the numeric algorithm used, as well as the data processing before and after each stage.

Since the technological semiconductor process simulation and electrical behavior characteristics used for the design and optimization of power semiconductor diode structures has been developed with the programs included within ***ISE-TCAD*** *–**I**ntegrated **S**ystems **E**ngineering-**T**echnology **C**omputer **A**ided **D**esign **AG**–* package, a detailed description of the programs, design and analysis is presented in the following sections.

3.5. ISE-TCAD Simulation System

Integrated Systems Engineering -ISE- is a provider of TCAD software products, covering the entire range from process simulation over device, circuit and system simulation. ISE was founded as a spin-off company of the Swiss Federal Institute of Technology Zurich (ETH) by several members of the Integrated Systems Laboratory (IIS). *Figure* 3.3 shows a block diagram of ISE simulation system.

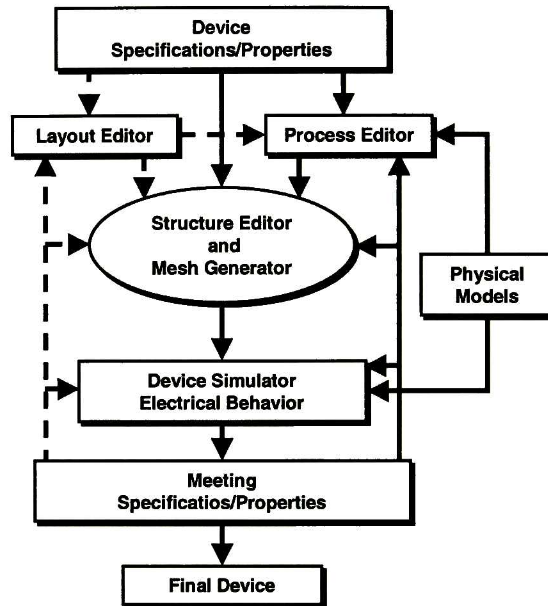


Figure 3.1: *Design flow using TCAD tools for power semiconductor device design.*

Figure 3.2 shows an advanced design process, where the simulated data are then passed to a parameters extractor which finds the devices best set of parameters given by a model template. Based on the chosen compact circuit model or designer requests a work flow tool will define a set of simulations that produces the outputs otherwise obtained by measurements. The flow results in a detailed circuit model including all parameters for the particular device. The compact model can now be used in a circuit simulator, like SPICE or SABER. Of course this methodology still requires real devices for calibration and validation, but the number of implemented designs can be remarkably reduced. This helps to save time and costs.

3.4. Review of CAD Simulation Tools

The design process of semiconductor devices discussed above to suit a complex set of physical and electrical specifications requires an advanced environment for design analysis. In an environment based on TCAD, tools for geometry generation by process simulation as well as for simulation of the physical models are required. Due to the different scales of simulation and the nature of the partial differential equations (PDEs) involved in the respective physical simulations, advanced meshing tools and data exchange facilities are also required in order to pipe simulation results from one tool to another [54].

Through the years, several computer programs have been introduced to solve equation systems which arise from problems in applied physics [55]. This section outlines the various software packages designed for the numerical solution of PDEs. Such packages can be divided into two main groups. The first group (Sub System/System) includes the design packages used for general-purpose applications, e.g., SPICE [56], SABER [57]. Due to the origin of these programs in the simulation of ICs, the semiconductor device models are not accurate, since their answer in the simulation does not consider important aspects of their structure and in consequence of their real behavior (e.g., thyristor, power rectifier diode by mentioning some). Therefore, these programs are not suitable for investigating the static and dynamic behavior of power semiconductor devices.

Device simulation is used to predict the electrical behavior of a semiconductor device from its structure. Device simulation often follows the process simulation mentioned above, which emulates the structure of a device. Using device simulation in this way allows designer to choose the process inputs which result in the desired device parameters, such as breakdown voltage, forward voltage drop, leakage current, etc. However, device simulation can also be applied to structures for which no known fabrication method exists. In this sense, simulation is used to explore new inventions in device design; if the new device is interesting, methods of fabricating it can then be explored. Device simulation is also used to understand unexpected device behavior, by providing a detailed picture of the internal electric field and carrier distributions when voltages are applied to the device.

Simulation plays an important role in power integrated device and circuit design. It is important to pointing out that the simulation of modern semiconductor power devices includes several added complexities that are not usually found in VLSI modeling [50]:

1. Modern power device technologies are as complex as VLSI technologies of similar dimensions, with added difficulties arising from float-zone substrate material and the excessively long and high temperature treatments.
2. Power devices operate in a circuit environment that has a drastic influence on the overall behavior of a switching system.
3. Thermal management plays a more central role in power device modeling. Often detailed simulation of the heating and cooling process including the thermal package is required.
4. Special physical mechanisms pertinent to power devices must be considered. Carrier-carrier scattering, lifetime engineering and traps dynamics are some examples.
5. Power devices are considerably larger than VLSI elements in order to obtain the required on- and off-state characteristics. The large size of these elements puts enormous requirements on the quality of the grid generators.
6. A realistic and accurate numerical simulation of the operating principles of power devices is only possible if the numerical stability of the codes and the physical models are well proven and stable.

3.3. Technology Computer Aided Design (TCAD) Methodology

In order to carry out state-of-the-art measurements of manufactured structures (empirical approach), one of the main goals of this thesis is to develop a design methodology that relies on a process, device and circuit simulation (a couple process) to design and to optimize power semiconductor diode structures. *Figure* 3.1 depicts a complete design flow for modeling power semiconductor devices developed in this work which is based on [51] and [52].

Via simulation programs, process simulation based on layout and technology information (process flow) provides a description of 1-D, 2-D or 3-D cross-sections device geometry and its doping profile. After the generation of a suitable grid, the electrical device behavior can be reproduced by a device simulator. For a correct prediction of device behavior the implementation of appropriate physical models is essential. After each change of a design parameter the designer uses the TCAD tools to evaluate the new performance of the device. If it does not meet the requirements he loops back to the appropriate step. Therefore, TCAD guided design methodology will have to include multiple levels of modeling hierarchy. Depending of the device to be simulated, for an accurate prediction of device operation, *figure* 3.1 has to be completed by the calibration of the simulators as well as the selection of appropriate physical and circuit models [53].

Chapter 3

TCAD Methodology: Physics-Based Power Rectifier Model

This chapter states the need for a TCAD design methodology that supports physical modeling for semiconductor devices. Consequently, it deals with a detailed description of the programs included within the simulation software of technological semiconductor process, and electrical characteristics behavior used in this thesis for the design and optimization of power semiconductor diode structures.

3.1. Introduction

RECENTLY new developments in semiconductor technologies and novel semiconductor devices have been guided by a numerical simulation approach. Numerical solutions of the set of equations defining the behavior of a system subject to external stimulations are indispensable when dealing with complex structures like realistic devices, in which it is impossible to obtain an analytical solution. Since at the present time semiconductor devices cannot be manufactured without having been simulated to predict the possible behavior that they will have in the reality, the simulation has become a standard tool in electronics. Moreover it allows a qualitative and quantitative analysis of the device.

However, one of the simulation problems is that the computer programs are often extremely complex to write, to use (including changes) and simply to understand what they are doing. Another drawback with computer models is the way that they are used. It is not difficult to get wrong results from simulations. Using the wrong input parameters, a mesh which is too coarse, or using a model outside its range of validity can each lead to convergence problems, or to incorrect answers. If the convergence is not reached, the code may stop before it reaches an accurate result. When a designer uses the simulation in a creative and appropriate way, and he has the knowledge to develop the strategy of simulation and interpret the results, simulation offers a powerful tool. An important point to notice about simulation is that the *optimum simulation* is one which captures the right physical process, and does so using a method which reflects the reality [49]. Therefore, the use of these tools requires very good physical background knowledge as well as the support from the vendor.

3.2. Simulation of Silicon Processing and Silicon Devices

Silicon chips are manufactured by an elaborate sequence of processing steps applied to a silicon wafer. The most common processing steps are the deposition and patterning of insulating or metallic layers, the implantation or diffusion of impurities to convert the neutral crystal into a positive (p-type) or negative (n-type) semiconductors and heat treatment to anneal crystal damages or grow insulating oxide. The development of a process which leads to a circuits of desired performance involves many decisions on processing conditions at each step in the process sequence. Traditionally such decisions have been made by trial and error. By using technology simulation tools, a process designer can bring the product to market faster by reducing development time, can reduce development costs by eliminating several trials and optimize circuit behavior while minimizing process sensitivity. Each process step involves a series of physical and chemical modifications of the wafer surface and underneath of the surface. The simulation of these steps is handled by the solution of differential equations for mass transport and material flow in the bulk, and by ballistic transport techniques on the surface.

2.5. Summary

In this chapter, the main requirements for the test and characterization of power rectifier diodes were discussed. A full review of the main diode forward recovery parameters (t_{fr}, and V_{PF}) and reverse recovery (t_{rr}, Q_{rr}, I_{PR}, V_{PR}) was presented, including the influence by external factors which govern the circuit operation (V_R, I_F, di/dt, di_F/dt, L_C, R and T_J).

The difference between inductive switching (ramp recovery) and resistive switching (step recovery) is the fact that under resistive switching, reverse current is constant during the initial phase whereas during inductive switching, the reverse current trough the diode falls at the rate determined by the external circuit. For sake of numerical convergence when a mixed-mode simulation tool is used, an ideal circuit fixture were presented, where the applied voltage is set by a time dependent voltage source through a piecewise linear function.

The evolution of the carrier distributions in power rectifiers diodes during the forward and reverse transient has also been considered. It has been shown that a critical current density, J_0, exist during at early time, immediately after the beginning of the forward transient. It has been shown that during ramp reverse recovery process, the peak reverse recovery current J_{PR} decreases as the high-level lifetime τ_a in the drift-region is reduced, this results in a smaller reverse recovery time, τ_{rr}.

the area under the reverse recovery current waveform and the initial stored charge is given by the product of the average drift-region concentration $\bar{n}$ and its thickness $2d$. Then [7]

$$\frac{1}{2} J_{PR} t_{rr} = Q_S = q\bar{n}2d = J_F \tau_a \tag{2.43}$$

By using equations (2.42) and (2.43), it can be shown that

$$t_{rr} = 2\tau_a \frac{J_F}{J_{PR}} = \frac{2b\lambda}{D_n} \tag{2.44}$$

Therefore by reducing the high level lifetime and by increasing the peak reverse current relative to the on-state current, a smaller reverse recovery time can be obtained. The time t_1 taken for the current to reach its peak reverse value can be solved for using equation (2.37) and the charge removed from the drift-region during the time interval from t_0 to t_1 using [7]

$$\frac{1}{2} J_{PR} t_A = Q_R(t_A) = \frac{1}{2} q\lambda\bar{n} \tag{2.45}$$

Substituting for $\bar{n}$ in this equation and solving for t_A

$$t_A = \frac{\tau_a \lambda}{2d} \frac{J_F}{J_{PR}} \tag{2.46}$$

The second portion of the reverse recovery occurs over a duration t_B which can be obtained by [7]

$$t_B = t_{rr} - t_A = \left(2 - \frac{\lambda}{2d}\right)\tau_a \frac{J_F}{J_{PR}} \tag{2.47}$$

In general, it is desirable to have a larger ratio of t_A to t_B in order to reduce the dJ/dt during the period t_B. Using the above equations, it can be shown that [7]

$$S = \frac{t_B}{t_A} = \left(\frac{4d}{\lambda} - 1\right) \tag{2.48}$$

Thus, a smaller value of λ will favor a softer reverse recovery waveform. Finally, if the reverse recovery current waveform is approximated as a triangle of base (t_A+t_B) and height I_{PR}, the reverse recovery charge is given by

$$Q_R = \frac{1}{2} I_{PR}(t_A + t_B) \tag{2.49}$$

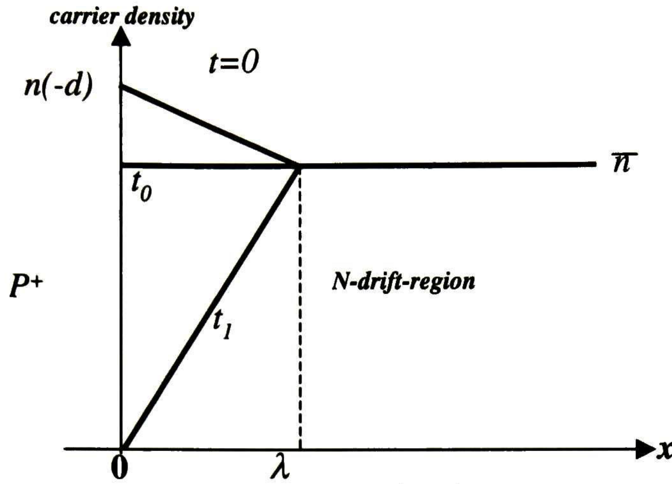


Figure 2.9: *Lineal carrier distribution within the* $P^+N^-N^+$ *rectifier during reverse recovery.*

$$\left.\frac{dn}{dx}\right|_{x=-d} = \frac{n(-d) - \bar{n}}{\lambda} \tag{2.38}$$

where $\bar{n}$ is the average drift-region electron/hole concentration. Combining expressions (2.37) and (2.38) to calculate the distance λ as a function of forward current J_F yields

$$\lambda = 2qD_n \frac{n(-d) - \bar{n}}{J_F} \tag{2.39}$$

At time t_1 the power rectifier begins to support the reverse voltage, thus the peak reverse recovery current J_{PR} is reached. In accordance with *figure* 2.9, the carrier density at the P^+-N^- junction becomes equal to zero at time t_1. Under the assumption that the carrier density varies linearly over the distance λ from 0 to $\bar{n}$, J_{PR} is given by [7]

$$J_{PR} = 2qD_n \frac{\bar{n}}{\lambda} \tag{2.40}$$

If J_F is determined by recombination in the drift-region from equation (1.19) in Chapter 1 it yields

$$\bar{n} = \frac{J_F \tau_a}{2qd} \tag{2.41}$$

Substituting equation (2.41) in (2.40)

$$J_{PR} = \frac{\tau_a D_n}{\lambda d} J_F \tag{2.42}$$

It can be seen from this equation that the peak reverse recovery current decreases as the high level lifetime in the drift-region is reduced. Since the charge removed during the reverse recovery process is

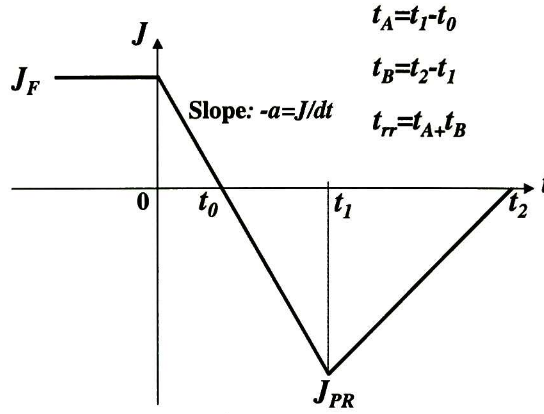


Figure 2.8: *Schematic of the reverse recovery current waveform.*

2.4.2. Ramp Reverse Recovery

In the following paragraphs a simplified analysis of the ramp reverse recovery of a power rectifier is presented. The starting point of this analysis is the assumption of a triangular turn-off current waveform between $t=t_0$ and t_2 shown in *figure* 2.8. Based on charge control analysis, the equation governing the stored charge per unit area $Q(t)$ due to the on-state current flow in the region $0<t<t_1$ is [48]

$$\frac{dQ}{dt}+\frac{Q(t)}{\tau_a}=J(t)=J_F-at \tag{2.34}$$

where $a=dJ/dt$ is the current ramp rate. Since the current density decreases linearly with time ($Q(t)/\tau_a \rightarrow 0$) [7]

$$Q(t)=\int_0^{t1} J(t)dt=\int_0^{t1}(J_F-at)dt \tag{2.35}$$

The solution of equation (2.35) is

$$Q(t)=J_F t-\frac{at^2}{2} \tag{2.36}$$

The carrier density in the on-state is the same as that derived previously for high level injection conditions (equation (2.26)).

It is assumed that during the ramp recovery, the carrier density decreases at the P^+-N^- junction while remaining relatively constant within the drift-region at a distance λ from the junction. The on-state current density is then given by [7]

$$J_F=2qD_n\left.\frac{dn}{dx}\right|_{x=-d} \tag{2.37}$$

with

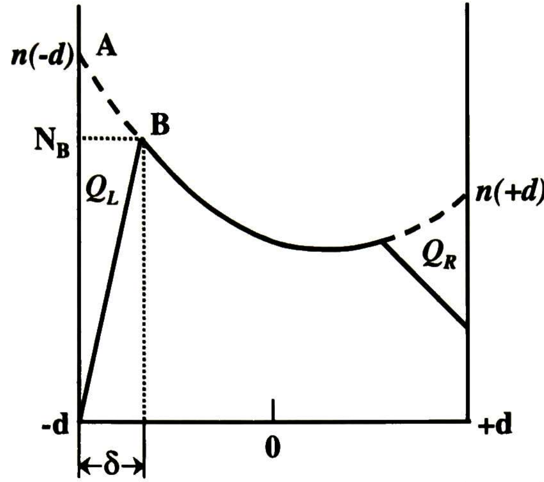


Figure 2.7: *Linear approximation for charge distribution at time t_L on the left- and right-hand of the drift-region.*

n(-d) and *n(+d)* can be obtained from equation (2.26). Solving it yields [22]

$$\frac{t_L}{\tau_a} = \left(\frac{J_F}{J_R}\right)^2 \frac{(1+(1/b))^2}{8} \coth\left(\frac{d}{L_a}\right)\left[1 + B\tanh^2\left(\frac{d}{L_a}\right)\right]^2 \tag{2.32a}$$

and

$$\frac{t_R}{\tau_a} = \left(\frac{J_F}{J_R}\right)^2 \frac{(1+b)^2}{8} \coth\left(\frac{d}{L_a}\right)\left[1 + B\tanh^2\left(\frac{d}{L_a}\right)\right]^2 \tag{2.32b}$$

Beyond the time t_R, the voltage across the diode builds up by the formation of these SCR on both sides of the device. The SCR regions then sweep toward each other as the carriers are continuously swept out of the drift-region. A detailed analysis of this process indicates that the voltage across the diode will be built up as the 3/2 power of time [22, 29]

$$V_{SCL} = \frac{2}{3}\sqrt{\frac{2}{\varepsilon_S q^3 \mu_p} \frac{b^2}{(b+1)^{3/2}} \frac{J_R^2}{n^{3/2}}} (t - t_L)^{3/2} \tag{2.33a}$$

and

$$V_{SCR} = \frac{2}{3}\sqrt{\frac{2}{\varepsilon_S q^3 \mu_n} \frac{1}{(b+1)^{3/2}} \frac{J_R^2}{n^{3/2}}} (t - t_R)^{3/2} \tag{2.33b}$$

where V_{SCL} and V_{SCR} are the voltage at the left and right sweep-out zones, respectively. Since b=3 for silicon, a comparison of the two components shows that the main part of the voltage is built up on the left hand side (P$^+$-side), e.g., 5.2 times as larger as the rate of build up on the right hand side (N$^+$-side).

Thus the charge removal from the anode side of the junction proceeds faster than from the cathode side. The current J_R will remain constant only until the concentration of holes reaches the background level in the base. Beyond this time, a space-charge region (SRC) will begin to develop at the anode (P^+-N^-) junction an a part of V_R will be supported by the diode. The current flowing in the circuit eventually falls off with time (see *figure* 2.3(a)). This produces a change in the excess minority carrier distribution within the drift-region which is given by equation (1.20) in Chapter 1, and is rewritten here as [29]

$$n(x) = p(x) = \frac{\tau_a J_F}{2qL_a}\left[\frac{\cosh(x/L_a)}{\sinh(d/L_a)} - B\frac{\sinh(x/L_a)}{\cosh(d/L_a)}\right] \tag{2.26}$$

where $L_a=(D_a\tau_a)^{1/2}$ is the ambipolar diffusion length, D_a the ambipolar diffusion constant and τ_a is the ambipolar lifetime in the drift-region. *Figure* 2.6(b) shows the associated excess minority carrier distribution (hole density in this case) and space-charge spreading in the drift-region at various points during the turn-off transient. The time at which the reverse current begins to decrease, t_L, can be derived with the aid of *figure* 2.7, which shows a linear approximation for the charge distribution at time t_L, on the basis of which J_R is given by

$$J_R = 2qD_p\frac{n(-d)}{\delta} \tag{2.27}$$

since δ is typically much smaller than d. From charge control [14],

$$J_R t_L = Q_L + Q_R = Q_L\left(1+\frac{1}{b}\right), \qquad \text{where} \qquad Q_L \cong bQ_R \tag{2.28}$$

here Q_L and Q_R are the charges that have been swept out on the left and right sides, respectively, b is the ratio of the charge removed from both sides. This ratio is determined by the ratio of the diffusion coefficients for electrons and holes. At low injection levels b=3, but at high injection levels the ratio b decreases as a result of carrier-carrier scattering and tends to unity [14]. If the curve section AB in *figure* 2.7 is approximated by a straight line, then [22]

$$Q_L \cong \frac{\delta \cdot q \cdot n(-d)}{2} \tag{2.29}$$

Combination of equations (2.27) and (2.29) gives [14]

$$t_L = q^2 D_p\left(1+\frac{1}{b}\right)\left[\frac{n(-d)}{J_R}\right]^2 \tag{2.30}$$

Similarly, the time t_R at which a SCR begins to form at the N^--N^+ junction can be derived under the assumption that the current is still approximately constant [14]

$$t_R = q^2 D_n(1+b)\left[\frac{n(+d)}{J_R}\right]^2 \tag{2.31}$$

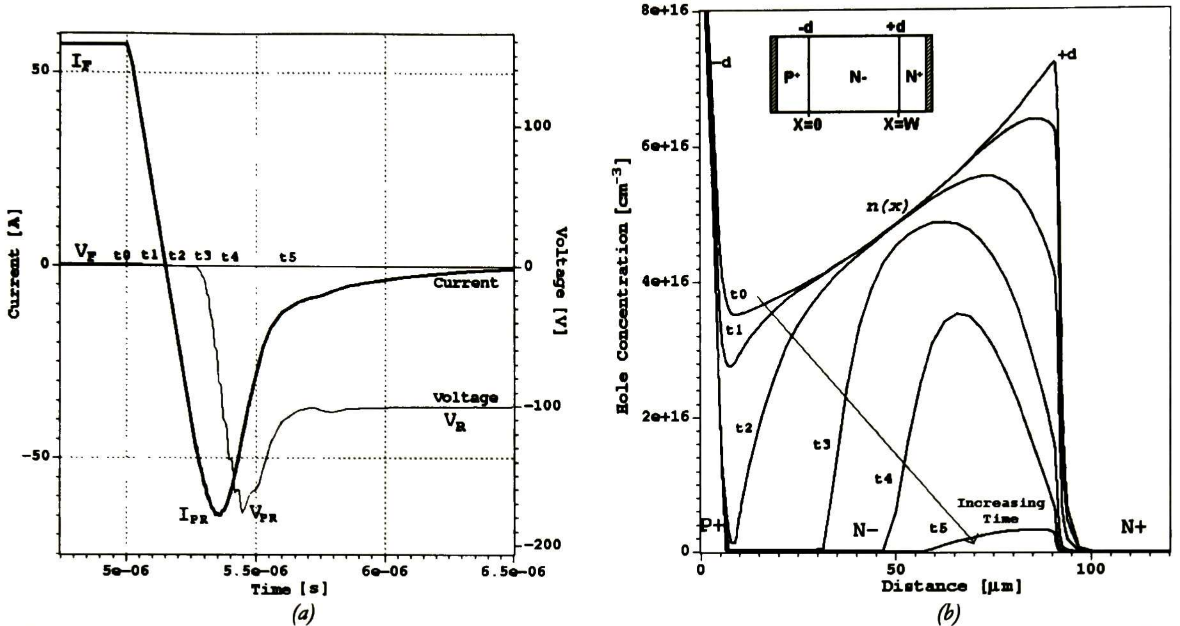


Figure 2.6: *(a)Reverse recovery characteristics and (b)evolution of associated excess minority carriers in the drift-region during reverse recovery.*

Phase 5 (Recovery Phase): This final phase starts when the voltage begins to fall reaching its steady-state reverse blocking value at $t=t_5$, while the current continues to drop to its leakage level. Some of failure modes in moderns fast rectifiers occurs during this phase and are mainly dependent on the remaining excess carrier near the N^--N^+ junction [47].

2.4.1. Step Reverse Recovery

Consider the case of a forward-biased power rectifier diode operating at high injection level with a forward current density J_F. At time $t=0$, if the voltage across the diode is reversed to a fixed value V_R with a resistance R connected in series with the diode (resistive switching), the current in the circuit will initially be limited to $J_R=V_R/(AR)$, where A is the diode's area. This external current is supported by the diffusion of holes from the middle N-base region into the P^+-region and the diffusion of electrons into the N^+-region (see insert in *figure* 2.6(b)). Thus, to maintain current continuity, the currents flowing out of the end regions must be equal. Thus

$$J_R = \frac{V_R}{A \cdot R} = qD_p \left.\frac{dp}{dx}\right|_{x=-d} = -qD_n \left.\frac{dn}{dx}\right|_{x=+d} \tag{2.24}$$

where $d=W/2$. Since for silicon the diffusion coefficient for electrons, D_n, is larger than that for holes, D_p, it follows that

$$\left.\frac{dp}{dx}\right|_{x=-d} > -\left.\frac{dn}{dx}\right|_{x=+d} \tag{2.25}$$

diode. Equation (2.20) predicts how the charge is injected at short times after the transient has begun. Obviously, as time progresses, the value of $f(x,t)$ will change, since substantial charge is stored near the high-low junction in the steady-state. The key turning point occurs when injected holes from the P^+-N^- junction reach the high-low junction (double injection occurs). This of course will increase $n(x,t)$, and increase $f(x,t)$. The injected charge will rapidly build up at the high-low junction after this time. This time can be estimated by dividing the middle region width W, by the drift velocity. Thus [43]

$$t_{di} = \frac{W}{\mu_p E_{bulk}} \tag{2.22}$$

Substituting equation (2.16) in (2.22), it can be written as

$$t_{di} = b\frac{qN_D W}{J_F} \tag{2.23}$$

where $b=\mu_n/\mu_p$ is the ratio of carrier mobilities discussed in Chapter 1. Certainly, even after $t=t_{di}$, diodes with $J_F<J_0$ will still have less charge injected at the high-low junction than diodes with $J_F>J_0$, but the difference will be less noticeable than $t<t_{di}$.

2.4. Reverse (turn-off) Transient

Reverse recovery of P-i-N diode structures (including P^+-N^--N^+ and P^+-P^--N^-) have been extensively studied in the literature, including the great diversity of carrier lifetime measurement techniques [13, 44, 43, 46]. *Figure* 2.6(a) shows typical diode current and voltage waveforms obtained from simulation results using ISE-TCAD software during reverse recovery. During Forward Conduction *FC*, the diode conducts a constant steady-state forward current I_F, and a fixed forward voltage drop V_F appears across the diode. The reverse recovery process is initiated when the diode is subjected to a reverse voltage V_R at $t=t_0$, a certain transient period elapses before the diode can reach its full Reverse Blocking *RB* state. This period can be divided into five phases [47]:

Phase 1 (Commutating Phase): This phase begins with the application of the reverse voltage V_R at $t=t_0$. The current drops at a rate di/dt until it reach the zero crossing point at $t=t_1$.

Phase 2 (Stored Phase): This phase starts after $t=t_1$ as the current turns negative. The phase ends at $t=t_2$ when the total excess carrier concentration at the P^+-N^- junction is reduced to zero. It can be noticed that the reduction in the minority carrier concentration near the P^+-N^- junction is more rapid when compared with the other end.

Phase 3 (Voltage build-up Phase): This phase marks the start of the *recovery period* at which the depletion region starts to form across the P^+-N^- junction sweeping out the remaining excess carriers from the drift-region. The voltage across the diode will increase at a rate dv/dt as the depletion region widens, until it reaches the value of the applied voltage V_R at $t=t_3$. Hence at that point $di/dt=0$ and the diode current reaches its peak value I_{PR}.

Phase 4 (Inductive Phase): This phase starts when the recovery current begins to fall from its peak value I_{PR}, while the voltage continues to increase until it reaches the peak value V_{PR} at $t=t_4$.

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Unidad Guadalajara

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