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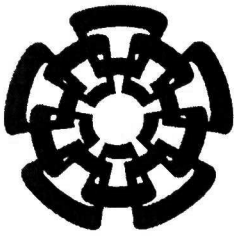

Centro de Investigación y de Estudios Avanzados
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Unidad Guadalajara

Topologías del DVR basadas en un convertidor matricial para mejorar la calidad de la energía en sistemas de distribución

Tesis que presenta:
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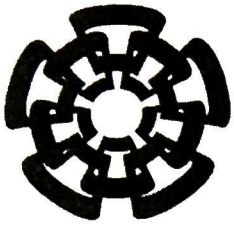
para obtener el grado de:
Doctor en Ciencias

en la especialidad de:
Ingeniería Eléctrica

Director de Tesis
Dr. Juan Manuel Ramírez Arredondo

CINVESTAV del IPN Unidad Guadalajara, Guadalajara, Jalisco, Febrero de 2011



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DVR's Topologies matrix converter-based for improving power quality in distribution systems

A dissertation submitted by:
José Merced Lozano García

For the degree of:
Doctor of Sciences

In the specialty of:
Electrical Engineering

Advisor:
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Dedicatoria

A mis padres, Concepción y Raquel, quienes constituyen el mejor ejemplo que pueda seguir, por su amor incondicional e incansable apoyo.

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A Dios, por permitirme continuar en este camino.

Resumen

El objetivo de la presente investigación es desarrollar un esquema de compensación de voltaje novedoso, capaz de mitigar algunos de los problemas más comunes concernientes a la calidad de energía en los sistemas eléctricos de distribución. Los disturbios suscitados en las redes de suministro de energía provocan variaciones en los perfiles de voltaje a lo largo del sistema especialmente en los nodos cercanos a la falla. Por otro lado, el incremento en la utilización de sistemas industriales automatizados, la conexión de fuentes convertidores basadas en electrónica de potencia, etc., generan una gran cantidad de componentes armónicos contaminando el sistema eléctrico. Estos eventos deterioran el rendimiento de equipos convencionales, ocasionan fallas en líneas de producción, provocan la desconexión de un gran número de usuarios y causan grandes pérdidas económicas en general.

Con el propósito de compensar tales condiciones adversas en el voltaje, en este trabajo de tesis se proponen dos nueva topologías para un Restaurador Dinámico de Voltaje (DVR) basadas en el convertidor matricial. Los esquemas propuestos incorporan la tecnología de la conversión de energía CA-CA y adquieren del sistema la energía de compensación requerida, lo que permite eliminar las desventajas que supone el uso de un enlace de CD y la necesidad de elementos de almacenamiento. La topología convencional del DVR se utilizada para generar los voltajes de compensación durante condiciones que involucran variaciones de voltaje balanceadas y desbalanceadas, además de voltajes distorsionados en el sistema. En la segunda topología, los voltajes de compensación se inyectan en el lado del sistema de suministro. Esta configuración permite que se mantenga un voltaje constante en las terminales de entrada del convertidor, resultando en una solución eficiente para la compensación de variaciones pronunciadas en el voltaje.

El control el DVR se logra mediante la combinación de un controlador *feed-back / feed-forward* y la estrategia de modulación propuesta, Modulación Directa en el Espacio Vectorial Modificada (MDSVM), desarrollada para generar los voltajes de compensación a través del convertidor matricial.

La implementación experimental del convertidor matricial está basada en interruptores de estado sólido IGBTs y el control se programó en un Procesador Digital de Señales (DSP). Se llevaron a cabo simulaciones numéricas en el programa PSCAD para validar las topologías propuestas, y además se presentan los resultados experimentales obtenidos a fin de confirmar el esquema de control.

Abstract

The objective of this research is to develop a novel voltage compensation scheme that can be able to cope with common power quality problems presented in power distribution systems. Disturbances occurring in the supply power networks or facilities in plants can cause variations in voltages profile throughout the system, especially in the nodes located close to the fault. On the other hand, the increasing use of industrial systems microprocessor-based, utility line-connected solid state power converters, etc., have polluted the power system with harmonic components. These events are reasons for failures in common equipment, tripping of computer-controlled industrial processing lines, power disruption for end users and economic losses in general.

In order to mitigate such voltages conditions, this dissertation proposes two novel DVR topologies based on the matrix converter. The proposed schemes include the AC-AC power conversion technology and acquire from the grid the necessary energy during the disturbance, which eliminates the drawbacks imposed by the use of DC-link passive devices and the need of energy storage components. The conventional DVR topology is used to generate the compensation voltages in conditions that involve balanced and unbalanced variations, and distorted supplied voltages. In the second topology, compensation voltages are injected on the supply-side of the system. This configuration permits to hold a constant input voltage for the converter, resulting in an efficient solution for deep voltage sags.

DVR's control is achieved by the combination of the feed-back / feed-forward controller and the proposed Modified Direct Space Vector Modulation (MDSVM) strategy, developed to generate the compensation voltages through the matrix converter.

The hardware implementation of the matrix converter is based on IGBTs and DSP control. Simulations in PSCAD software have been carried out to verify the validity of the proposed topologies, and prototype experimental results are provided to confirm the control scheme.

Contents

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List of Acronyms

EPS	Electric Power System
CUPS	Custom Power System
DVR	Dynamic Voltage Restorer
SMES	Super Magnetic Energy Storage
MDSVM	Modified Direct Space Vector Modulation
IGBT	Insulated Gate Bipolar Transistor
DSP	Digital Signal Processor
CEA	Canadian Electric Association
EPRI	Electric Power Research Institute
NPL	National Power Laboratory
PCC	Point of Common Coupling
ANSI	American National Institute
IEEE	Institute of Electrical and Electronics Engineers
ITIC	Information Technology Industry Council
CENELEC	European Committee for Electrotechnical Standarization
IEC	International Electrotechnical Commission
IEEE-IAS	Institute of Electrical and Electronics Engineering, Industry Application Society
NEMA	National Electric Manufactures Association
FACTS	Flexible Alternating Current Transmission Systems
SSSC	Static Synchronous Series Compensator
TSSC	Thyristor Switched Series Capacitor
TSSR	Thyristor Switched Series Reactor
SSG	Static Synchronous Generator
SVG	Static Var Generator
STATCOM	Static compensator
TCR	Thyristor Controlled Reactor
TSC	Thyristor Switched Capacitor
UPFC	Unified Power Flow Controller
DSTATCOM	Distribution Static Compensator
UPQC	Unified Power Quality Conditioner
NCC	Naturally Commutated Cycloconverter
VeSC	Vector Switching Converter
SCR	Silicon Controlled Rectifier
THD	Total Harmonic Distortion
FRD	Fast Recovery Diode
CSC	Current Switch Clamped

VSI	Voltage Source Inverter
PWM	Pulse Width Modulation
SVM	Space Vector Modulation
ISVM	Indirect Space Vector Modulation
DSVM	Direct Space Vector Modulation
ADC	Analog / Digital Converter

CHAPTER I

Introduction

1.1 Introduction and Motivation

Nowadays, electricity supply industry has been experienced extraordinary changes mainly aroused by the imminent scarcer of natural resources, the continuously energy demand increments and the quality of delivered energy concerned. All these reasons, together with a variety of environmental and regulatory pressures that prevent the building of new power generating plants and transmission lines, are taking the power systems to operate close to their stability and thermal limits.

Among the actual issues related to electric power systems (EPS's), the term electric power quality has gained considerable attention by both electric suppliers and end users. From the standpoint of utilities, the major concern relies on fact that contemporary devices and equipment (electronic-based systems) being used by industrial and commercial customers are more sensitive to power quality variations than equipment used in the past. From the power grid point of view, the increment of electronic loads becomes important sources of power quality degradation, which causes a growth in the application of passive devices as capacitors for harmonic filtering and power factor correction. These capacitors change the system impedance resulting in possible resonance, which can magnify transient disturbances and harmonic distortion levels.

Power quality delivery refers to the ability of transmission and distribution systems to deliver the electric power to any point of consumption in the amount and quality demanded by the customer. Every system has different influence on the level of the quality of delivery. For example, a failure in a transmission component may lead to subsequent loss in distribution power. A failure in distribution components only causes local losses in costumer loads. Whereas problems related to power transmission systems and power distribution systems are all fundamental from power quality point of view, only some distribution systems issues are considered in this dissertation.

Deterioration of energy at distribution levels can be caused by natural causes: faults or lightning strikes in feeders and equipment failure, by feeder line operation or loads. For instance, power electronic based loads, switching on/off large loads etc. When one of this events occurs somewhere in a distribution system, the voltage is affected throughout it. Therefore the term power quality includes two important aspects [1.1]:

- Voltage quality. Involves rapid changes, harmonics, interharmonics, imbalance, etc.
- Supply Reliability. Involves phenomena with longer duration, voltage sags, swells, interruptions, etc.

As stated above, in front of the importance acquired by power quality topics in EPS's there is a general agreement by researchers worldwide, that novel power electronics equipment is a potential substitute for conventional solutions, which are normally based on electromechanical technologies that have slow response and high maintenance costs [1.2]. As conventional devices are being inefficient for actual power delivery problems, many researchers have focused their efforts in the developing of novel control strategies and operational techniques in order to replace them [1.3]. In the present investigation two novel topologies are proposed for a Custom Power System (CUPS) device, with the purpose of mitigate some of the common power quality problems found on electric distribution systems.

1.2 Justification

As mentioned above, the actual technological advance achieved in the power electronics area has allowed the optimization of a diversity of components inside the EPSs, particularly in the energy conditioning field. On the other hand, this tendency has given rise to the appearance of new issues in power transmission and distribution systems, which implies a huge challenge. One of the main concerns in which researches around the world have been focused on, is the power quality topic. The adverse effects caused by sags or swells in the manufacture process and sensitive loads have been described in several publications [1.4]-[1.7]. Likewise, the voltage harmonics problematic has been broached in manifold publications [1.8]-[1.10]. In general, power quality issues become direct factors of economic losses. Hence, the development of Custom Power Systems for improving the power system operation is imperative.

The series compensation device DVR (Dynamic Voltage Restorer) was introduced for voltage sag mitigation and has been adopted as a common solution to the problem. Since its introduction in 1994, several topologies have been developed, along with different control

methods and with harmonic compensation purposes [1.11]-[1.14]. While DVR topologies with energy storage are highly favored to compensate deep level voltage sags, this type of systems has significant drawback regarding complexity and overall cost.

Most of the DVR topologies presented in the literature share one specific characteristic: the DC-link. In order to eliminate the drawbacks imposed by the use of DC-link passive elements, some researchers have focused their efforts in develop novel topologies based on AC-AC power conversion [1.6], [1.15]-[1.8]. The advantages of utilizing AC-AC converters as an alternative to the use of DC-link converters are listed:

- The presence of huge electrolytic capacitors or another external storage system as batteries, super-capacitors or super magnetic energy storage (SMES) is not required.
- Reduced maintenance requirements
- High Power density
- Reduced harmonic level of low frequencies in the input current

Among the AC-link conversion topologies aimed to operate as a voltage compensator, the matrix converter offers the next operative advantages:

- Theoretically a non limited output frequency
- High quality output voltage and input current waveforms
- Controllable input power factor
- Four quadrant operation
- Excellent dynamic response
- Compact design

A further analysis of matrix converter is presented along with novel DVR topologies based on this device.

1.3 Objectives and Contributions

This dissertation proposes a Modified Direct Space Vector Modulation (MDSVM) strategy to control the matrix converter voltage generation which is developed from the analysis of voltage and current Park vectors in the complex space, considering a set of three phase unbalanced input voltages. The precise control of the reference vectors allows generating a set of controllable voltages in magnitude, phase and frequency. Control of the phase voltages are accomplished independently, characteristic that allows the matrix converter to operate as a voltage compensator which results in the proposition of two novel DVR topologies based on the AC-AC converter.

Through the proposed DVR topologies, this dissertation addresses the more common power quality problems, in particular sags, swells, unbalanced and harmonic voltages. Together, they account for more than 90% of the power quality disturbances affecting most commercial and industrial customers. Simulation and experimental results are provided to verify the proposed configurations. The hardware implementation of the matrix converter is based on IGBTs and DSP control.

Taking into account the operative features achieved through the combination of the feed-back-feed-forward controller and the MDSVM strategy, the proposed DVR topologies become an economical effective solution to overcome the power quality problems in electric distribution systems.

The main contributions of current research work are summarized as follows:

- The mathematical development of the MDSVM to control the matrix converter operation
- Design of two novel multi-functional DVR topologies based on the matrix converter
- Numerical evaluation of the proposed DVR topologies dynamic performance through a detailed model implemented in PSCAD software
- Implementation of a laboratory-scale prototype of the matrix converter based DVR

1.4 Thesis Outline

The thesis organization is as follows:

Chapter II. A brief overview of the power quality issues including literature surveys about voltage disturbances, related industrial standards, and mitigation schemes are presented. This chapter is focused on the more common power quality problems: sags, swells, unbalanced and harmonic distortion in voltages.

Chapter III. This chapter presents the matrix converter state-of-the-art. A historical review is carried out based on the literature, towards matrix converter introduction. Then, theoretical and practical basic concepts are reviewed to completely understand the AC-AC converters operational principle, emphasizing advantages and drawbacks of this technology, towards matrix converter practical implementation. Finally, commutation techniques and modulation strategies are analyzed and compared.

Chapter IV. In this chapter the proposed MDSVM strategy is developed which is one of the main objectives of this dissertation. The MDSVM technique is based on the direct DSVM modulation in which the output voltage and input current are controlled by means of magnitude and phase modification of the reference vectors in the complex space. Simulation and experimental results over various adverse conditions are presented to verify the strategy's effectiveness.

Chapter V. In chapter V, this research proposes two DVR's topologies for voltage compensation incorporating the matrix converter technology. The DVR's operational principle is presented, along with a comparison of the conventional topologies. After analyzing different schemes, and according to the objectives above mentioned, the final topologies are justified and the basic configurations are presented. To efficiently mitigate the voltage disturbance, a voltage controller is designed and explained. Finally the state-space equations for both system configurations are derived.

Chapter VI. Simulation results of voltage disturbances are presented to show the fast control response and the well-regulated output voltage using the proposed scheme. Experiments have been carried out to demonstrate the validity of the proposed topologies and results are presented in this chapter. Likewise, the hardware configuration is briefly explained.

Chapter VII. The conclusions and contributions resulting from this research work are presented in this chapter. Recommendations for future research on this topic are also provided.

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CHAPTER II

Voltage Disturbances and Mitigation Devices

Nowadays, there is an increasing demand for high quality and reliable power. One important reason for that is that all electrical devices are prone to failure or malfunctioning when they are exposed to one or more power quality problems. The concept of power quality at distribution level refers to maintaining a near sinusoidal power distribution bus voltage at a rated magnitude and frequency.

This chapter introduces the concept of power quality, reviewing the common terms and the typical characteristics of some voltage disturbances. In addition, a brief comparison of previous work in power electronics-based equipment for voltage compensation is exposed.

2.1 Power Quality Issues

The power quality term is commonly used to denominate the shortcomings present in transmission and distribution systems. This concept implies supply availability, reliability and voltage quality in the power supplied to the customers. Power quality degradation is inherently related to any failure of equipment due to deviations of the line voltage from its nominal characteristics, which often results in industrial process interruption causing substantial economic losses [2.1].

The principal phenomena concerned in power quality are [2.2]:

- Harmonics and other departures from the intended frequency of the alternating supply voltage
- Voltage fluctuations, especially those causing flicker
- Voltage dips and short interruptions

- Unbalanced voltages on three-phase systems
- Transient over-voltages, having some of the characteristics of high-frequency phenomena.

Fig 2.1 shows a general classification of power quality issues originated in the power distribution system and within the end-user. As in this thesis voltage based compensation is considered, the adverse effects of distribution system voltages are briefly revised in the next sections.

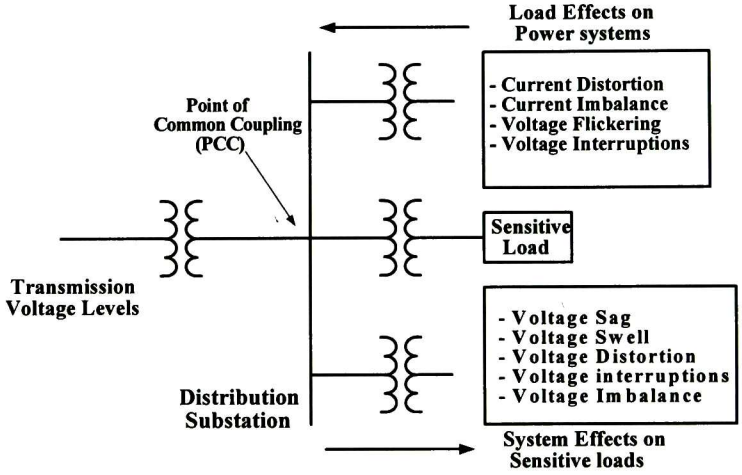

Figure 2.1. Sources of power quality problems

2.1.1 Voltage disturbances in distribution systems

A few years back, the main concern of consumers of electricity was reliability of supply. However, actual sensitive loads and modern communications needs a reliable supply with high quality voltage, that means AC line voltage supply with a pure sine wave of fundamental frequency and at rated peak value. Achieving such power delivery conditions is very difficult in electric distribution systems because to all the failures generated within the system are associated problems of voltage variations and power interruptions. Unfortunately, at the present time most of the loads in the distribution system are not tolerant to large voltage fluctuations.

There are many ways in which the lack of quality power affects customers [2.3]. Voltage dips can cause loss of production in automated process, and can also force a computer system or data processing system to crash. Sustained overvoltage can cause damage to household appliances, industrial equipment failures due to insulation breakdown, magnetic

saturation, and resultant harmonic generation. Under-voltages may cause degradation in the performances of the loads such and induction motors, light bulbs, etc. Voltage imbalance can cause temperature rises in motors. Harmonics can cause losses and heating in transformers, electromagnetic interference and acoustic noise. In conclusion, it is crucial to maintain a power quality high standard. Thus, is necessary to have a vast knowledge of the actual phenomena which may cause the problems. The main voltage disturbances are summarized in Figure 2.2.

Among various power quality problems, the majority of events are associated with either a voltage sag or a voltage swell, and they often cause serious power interruptions.

Voltage sag is a momentary decrease of the voltage rms value with the duration of a half a cycle up to many cycles. According to the Canadian Electrical Association (CEA) and the Electric Power Research Institute (EPRI) surveys, a voltage sag is defined as being less than 92% and 90% of nominal voltage, respectively [2.4]-[2.6]. For the CEA, a swell condition can be defined as the voltage level greater than 104% of nominal voltage, while that of the EPRI is 110%. In the National Power Laboratory (NPL) survey, the voltage range of 106% to 110% of nominal voltage is considered to be a voltage swell event. A revision of the data collected concerning on voltage disturbances indicates a predominant presence of voltage sags in electric power systems. In [2.7] it can be seen that voltage sags events defined by 0% to 87% of nominal voltage comprise 68% of power disturbances registered by the NPL and 93.3% of total events registered by the EPRI.

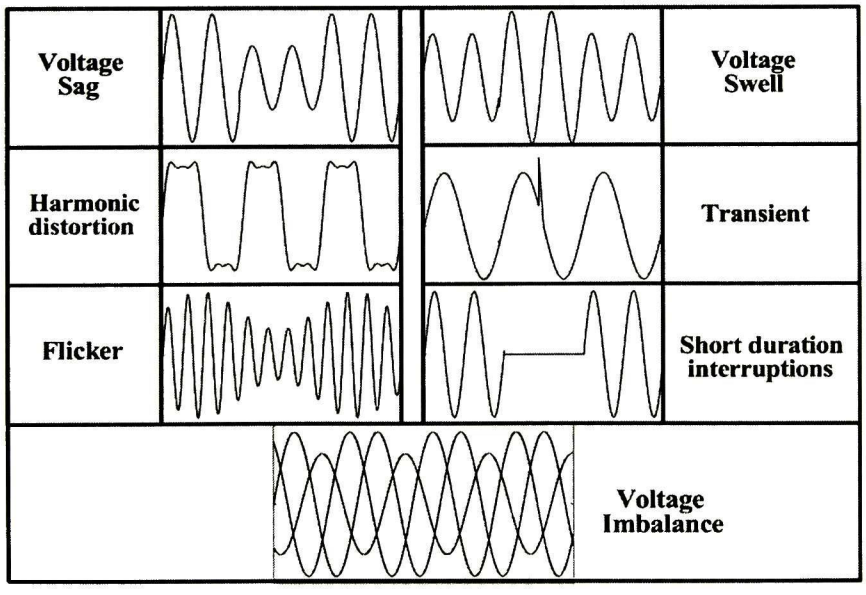

Figure 2.2. Voltage disturbances

Besides the above surveys, many papers have reported power quality surveys. The data presented in [2.8] indicates that most of faults are single-line to-ground fault, where 2% of all faults correspond to voltage sags with the remaining amplitude down to 40-50% of nominal value, and that most of these faults last for less than 2 seconds. Long-term interruptions (2 seconds to ten minutes) proved to be rare, accounting for an additional 4% of all faults. Similar data have also been recorded in a survey of Canadian power systems in 1997 [2.9]. According to [2.10], switching power supplies, industrial control relays, contactors, solenoids, adjustable-speed motor drives and thyristor controlled rectifiers are all susceptible to short term voltage sags.

2.1.2 Harmonic distortion

Another power quality issue which recently has receives considerable attention are the power systems harmonics. The increasing use of industrial systems microprocessor based, utility line-connected solid-state power converters, etc., has prompted growing concern over this aspect. A widely definition uses for harmonics establish that: "*harmonics are sinusoidal voltages or currents having frequencies that are integer multiples of the frequency at which the supply system is designed to operate*" [2.11].

Ideally, three-phase voltages are balanced and with constant rms (root mean square) value and frequency in each phase. Thus, when an electric load is linear, the voltage and currents are perfect sinusoids. However, the popularity of electronic components and other kind of non-linear loads makes these waveforms become distorted. A common non linear load is an ac induction motor drive, in which the most significant harmonic currents injected into the ac supply include the 5^{th}, 7^{th}, 11^{th}, and 13^{th} harmonics. When source inductance is taken into account, circulation of harmonic currents in the ac system results in voltage distortion at various points in the ac system. The distorted voltage waveform affects the operation of both the nonlinear load and other linear and nonlinear loads connected to the same bus, or PCC, or adjacent buses, as Fig 2.3 shows.

Harmonic voltages impact on power systems consists in the generation of harmonic currents. When these currents flow through magnetic devices such as energy transformers, motors, etc., can generate excess heat, additional losses and shorten devices' lifetime. On the other hand, harmonics or interharmonics with frequencies within hearing range, can produce interferences on telephone lines via inductive coupling, as well as over-current relays and power brakers malfunctioning due to skin effect [2.12]-[2.13]. Additionally to problems mentioned above, there exists other kind of events related to harmonics that have impacts in power system capacitors. Although a capacitor is not a harmonic source, it can provide the loop to harmonic currents, creating the conditions for repetitive over-voltages in capacitor banks increasing the temperature, accelerating age, and even explode. In

addition, if capacitors are applied at locations having large adjustable-speed drives, the potential to resonance problems must be considered.

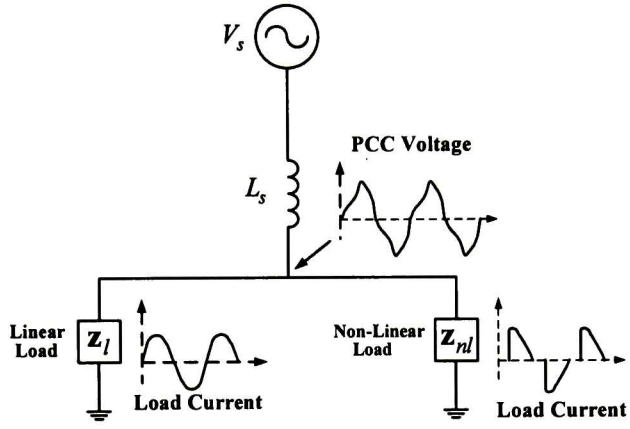

Figure 2.3. Voltage harmonics propagation

2.1.3 Voltage imbalance

In three-phase systems, load imbalance could be caused by unevenly distributed single-phase load or by balanced three-phase load running at a fault condition, such as phase open or short fault.

An unbalanced three-phase voltage source applied to three-phase motors causes the appearance of a negative sequence current which increases the motor's internal losses, heating it up. If the motor is running at near rated loads, then this could cause the motor overheat and could be severely damaged. Table 2.1, displays the effects of unbalanced phase voltages applied to class A and class B three-phase motors running at rated loads. In addition to motor damage, voltage imbalance in three phase systems can cause malfunctioning of the electronic equipment connected [2.16].

Table 2.1. Effect of voltage imbalance on motors at rated load

Voltage Imbalance (%)	0	2	3.5	5
Negative sequence current (%)	0	15	27	38
Increase in losses (%)	0	9	25	50
Class A Temperature raise (°C)	60	65	75	90
Class B Temperature raise (°C)	80	85	100	120

2.2 Power Quality Guidelines and Standards

Currently, several engineering organizations and standard bearers in several parts of the world are spending a large amount of resources to generate power quality standards. The American National Standards Institute (ANSI) and the Institute of Electrical and Electronics Engineers (IEEE) have established several guidelines concerning major power quality problems.

Regarding voltage tolerance, it depends on the specific application. That is the main reason why it is almost impossible to develop guidelines and operative standards that can encompass acceptable limits regarding voltage levels in distribution systems. Companies that build sensitive equipment should provide acceptability curves for the equipment they produce. Anyhow, curves as CBEMA [2.17], and Information Technology Industry Council (ITIC) curve [2.18], Fig. 2.4, suggest a guideline for voltage quality in power distribution systems serving main computers, and it can become an industry reference for acceptable voltage tolerance. This curve specifies the voltage dip magnitude and the duration of the voltage sag for 120 V single-phase applications. This curve is useful for providing general insight into acceptable voltage quality.

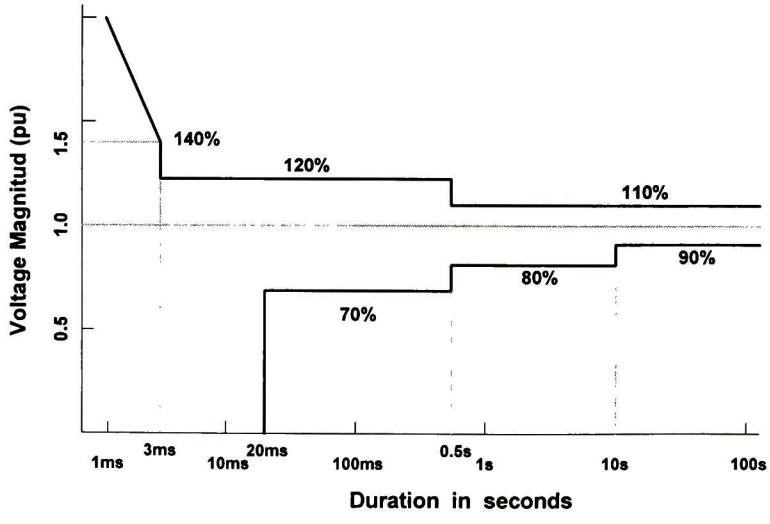

Figure 2.4 ITIC curve

About the harmonic distortion presented in distribution systems, several organizations as CENELEC (European Committee for Electrotechnical Standardization), IEC (International Electrotechnical Commission) and IEEE-IAS (Institute of Electrical & Electronics Engineering, Industry Application Society), have established professional committees to investigate the harmonic distortion impacts. Among the standards developed to supervise

harmonic distortion issues, the IEEE-519 guide for evaluation of the power system harmonic level issued in 1992 [2.15], is the most comprehensive.

Summaries of the acceptable amount of harmonic distortion presented in distribution systems are given in Table 2.2.

Table 2.2. Voltage distortion guidelines for power systems

Power system voltage level	*Dedicated Power System	General Power System
Medium Voltage 2.4 kV to 69 kV	8%	5%
High Voltage 115 kV and above	1.50%	1.50%

* A dedicated power system is one supplying only converters or loads that are not affected by voltage distortion.

Where voltage distortion percentage is defined as,

$$\%_{distortion} = \left(\sqrt{\frac{\sum_{h=2}^{\infty} V_h^2}{V_1^2}} \right) 100 \tag{2.1}$$

where V_h is the amplitude of the h^{th} harmonic voltage and V_1 is the amplitude of the fundamental voltage.

Finally, referring to voltage imbalance, there are several ways to define it. One definition is given in NEMA standard MG1 [2.14], where voltage imbalance is expressed as a percentage according to,

$$\%_{unbalance} = \frac{3\left(V_{a,b,c\max} - V_{a,b,c\min}\right)}{V_a + V_b + V_c} 100 \tag{2.2}$$

where $V_{a,b,c\max}$ is the maximum rms phase voltage, and $V_{a,b,c\min}$ is the minimum *rms* phase voltage. NEMA MG1 sets a voltage imbalance guideline of no more than 1% in order to prevent damage to sensitive loads.

2.3 Power Electronics Applications in Power Systems

The evolution taking place in the electricity supply industry is heading toward maximizing existing transmission and distribution resources, with high levels of stability and power quality. This trend points in the direction of power electronics [2.19]. Two kinds of power electronics applications have gained importance in power systems, and now are already well defined: active and reactive power control, and power quality improvement.

The first application area is for arrangements known as Flexible Alternating Current Transmission Systems (FACTS), where the latest power electronic devices and methods are used to control the transmission side of the electric network. The second application area is for devices known as Custom Power System (CUPS), which focus on the distribution system supplying the energy to end-users and is a technology created in response to reports of poor quality of supplied energy.

2.3.1 FACTS controllers

The FACTS concept was introduced by Narain G. Hingorani [2.20]-[2.21] at the end 80's, to face with the requirement of improving the transmission system operation. According to IEEE, FACTS controllers are defined as [2.22]: *Alternating current transmission systems which use power electronics-based static compensators to improve the controllability and increase the power transfer capability.*

FACTS controllers' operational principle is based on the modification of electric system parameters such as: transmission line impedance, voltage magnitude and phase angle in one system node. Some of the advantages achieved by FACTS controllers are [2.23]-[2.24]:

- Higher control on power flow.
- Voltage regulation on system nodes.
- Increase the system transient stability margins.
- Damp system oscillations, preventing equipment damage and increasing power transmission capability.
- Allow reliable interconnections between companies and neighbor regions.
- High power flow transfer capability between controlled interconnected systems.

According to the connection, FACTS controllers can be divided into [2.25]:

- Series connected devices.
    - Static synchronous series compensator (SSSC).
    - Thyristor switched series capacitor (TSSC).
    - Thyristor switched series reactor (TSSR).

- Shunt connected controllers
    - Static synchronous generator (SSG).
    - Static var generator (SVG).
    - Static compensator (STATCOM).
    - Thyristor controlled reactor (TCR).
    - Thyristor switched capacitor (TSC).

- Combined controllers
    - Unified power flow controller (UPFC)
    - Shift phase transformer

Each FACT device is designed to carry out specific control functions within the power systems. At present, an extensive bibliography related FACTS technology does exist [2.25]-[2.27].

2.3.2 Custom Power System (CUPS) devices

As with FACTS devices in transmission systems, power electronics devices can be applied to the power distribution systems to increase reliability and the quality of power supplied to the customers [2.28] –[2.29]. The devices applied to the power distribution systems for the benefit of customers are called Custom Power Systems.

Custom power devices are basically a compensating type, used for active filtering, load balancing power factor correction and voltage regulation. These devices usually include VSCs controlled by various control strategies and depending on the topology can be divided in three major types: current, voltage and combined compensation. Selected devices pertinent to CUPS technology are:

- Distribution Static Compensators (DSTATCOM) [2.30]. This device can complete current compensation, power factor correction, harmonic filtering, load balancing and also voltage regulation.

- Dynamic Voltage Restorer (DVR) [2.31]. The DVR is a device implemented in low and medium voltage to perform voltage based compensation as voltage harmonics filtering, voltage regulation and balancing. The conventional DVR topology is constituted by a passive storage element feeding a voltage inverter through a DC-link. In recent years the DVR has gained acceptance among industrial consumers as an efficient and economic solution to mitigate voltage disturbances on power feeders. However, despite its operational advantages exhibited, DVR capabilities are conditioned by the energy storage device used. As the main objective of this thesis is to develop a novel DVR topology, more details about DVR operational principle, configuration and control techniques are presented in Chapter V.

- Unified Power Quality Conditioner (UPQC) [2.32]-[2.33]. The combination of current and voltage compensation in distribution systems is referred to as the UPQC. The conditioning functions of the UPQC are shared by the series and shunt compensators; while its series compensator performs harmonic isolation between supply and load, voltage regulation and voltage flicker/imbalance compensation, the shunt compensator performs harmonic current filtering and negative sequence balancing as well as regulation of the DC-link voltage.

2.4 AC-link Power Converters

The second generation of FACTS controllers is based mainly on DC-link voltage source converters [2.34]-[2.35]. However, some advances on AC-AC converter-based controllers have appeared recently [2.36]-[2.40], being a novel choice for power conditioning and power flow control.

According to the operating principle, the AC-AC converters can be classified as follows [2.36]:

- Direct AC-AC converters.
- AC-link converters.
- AC-DC-AC converters.

Since the AC-DC-AC converter requires a DC-link it will not be considered as part of the AC-Link technology and therefore will not be analyzed here. The other two types of configurations are briefly presented, emphasizing their main characteristics.

2.4.1 Direct AC-AC converters

Direct AC-AC converters belong to the static frequency changers devices. The term static frequency changer is applied to electric circuits integrated by semiconductor switches and able to convert electric power with a frequency ω_1, at the input supply system terminals, to electric power with a frequency ω_2, at the load terminals. Static frequency changers can control frequency and voltage magnitude at load terminals without the need of transformers, just based on the static power switches control. Thus, load voltage is synthesized from segments of input voltage.

According to the switches' technology they can be divided in:

- *Naturally Commutated Cycloconverters (NCC).*

A three-phase to three-phase NCC is illustrated in Fig. 2.5 [2.41]. It requires naturally commutated back-to-back three-phase inverters for each output phase. Depending on the load current direction, the positive or negative inverter will be switched on. In each inverter, the operational mode (rectifier or inverter modes) is determinate by the output voltage sign.

Employing NCCs output voltage and frequency can be controlled but it is not possible to regulate input power factor. Traditionally, NCCs have been applied as drivers for high power AC motors, where no other kind of drive can be used. Concerning its drawbacks, next limitations can be pointed out:

- Output frequency of approximately 0.33 of input frequency
- Complex control strategy
- High number of thyristors
- Output voltages and input currents with a high level of harmonic content
- Input power factor depending on load power factor.

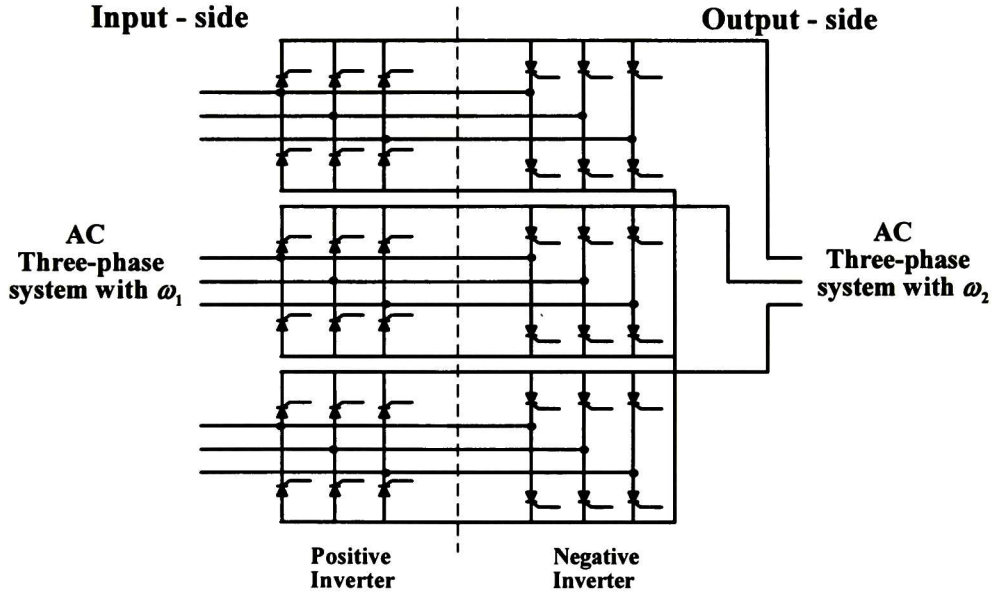

Figure 2.5. Three phase-to-three phase NCC

- AC-AC *Matrix converters.*

Matrix converter devices are based on the forced-commutation principle, for which utilize power bidirectional switches commutating at high frequencies. The matrix converter denomination is due to its structure resembles a power cells matrix with

"*m*" input lines and "*n*" output columns, as can be seen on Fig 2.6. The matrix converter belongs to the *Unrestricted Frequency Changers* family, since the output frequency is only restricted by practical aspects. On the other hand, a major restriction imposed to this converter is related to its transfer voltage ratio, which is limited to 0.866 times the input voltage. Another important limitation in matrix converter implementation is the lack of commercially available power bidirectional switches; however, this disadvantage can be overcome through the use of unidirectional switches configurations. By connecting a LC passive filter at the input terminals of the converter, input current harmonics are attenuated and the commutation process is improved.

Three remarkably aspects make this kind of technology very attractive:

i) Unrestricted output frequency
ii) Input current with low harmonic content
iii) Controllable input power factor

Due to the matrix converter advantages, it is a good option for the following applications:

AC motor driver in areas where physical size is to be considered or operation under adverse environments is required.
Link-converter between non-conventional electric sources and the AC power supply system.
Interconnection of power systems with different frequencies.
- Voltage disturbances compensation in distribution systems.

2.4.2 AC-link converters

AC-link converters are converters without frequency change capability but with simpler topologies than AC-AC direct converters. They can be transformers assisted or not. The most important AC-link converters' applications are focused on power flow control and voltage regulation. The AC-link converter principle is the high frequency chopping of an AC signal with constant duty cycle, in this way the converter can modifies the amplitude of the fundamental frequency component. The output signal contains such modified component plus high frequency components due to the switching.

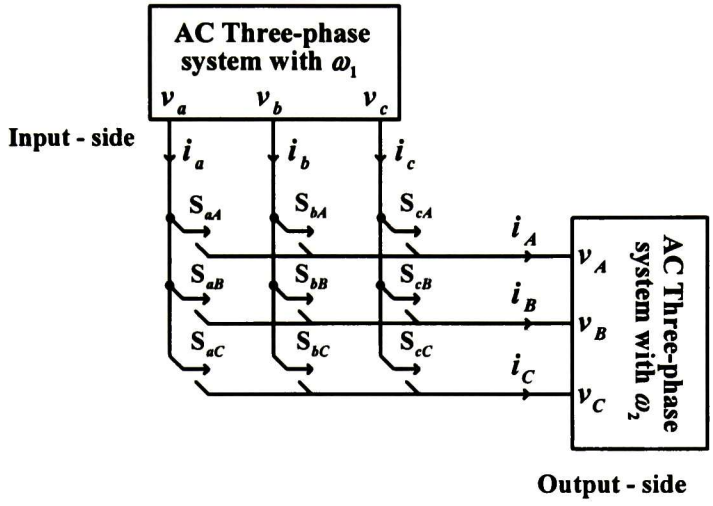

Figure 2.6. Three phase-to-three phase matrix converter

Based on o the well known DC-DC energy conversion strategy, AC-link converters have emerged as a novel solution for compensation voltage applications. For instance: buck, boost and buck-boost topologies. Fig 2.7 shows a one-phase AC-link buck and boost converters. In these topologies AC-link converters consists of two static power switches per phase and passive elements such as inductors and capacitors, used for increasing or decreasing voltage magnitudes. Since in AC-link converters current flows in both directions, bidirectional switches have to be taken into account. In Fig. 2.7, switches S1 and S2 operate in a complementary way, being necessary to provide a dead-time between switching operation to avoid the risk of short-circuits.

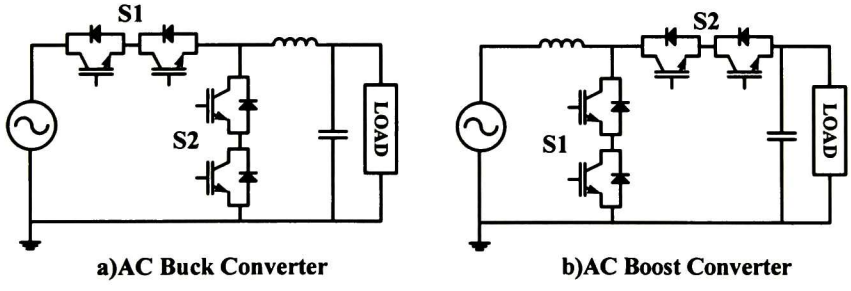

Figure 2.7. AC-AC voltage regulator topologies

For voltage compensation purposes with the previous topologies, a transformer would be necessary to reject steps down and voltage swells variations. Then the topology with the AC-link buck type converter with a transformer at the output terminals would be similar to the traditional DVR configuration just replacing the energy storage device and the DC-AC

inverter with the AC-link converter. In this way, by reducing the number of elements, the overall cost of the system is reduced as well. Along with the topologies presented, other topologies with AC-link converters have been proposed for voltage sags compensation [2.19], [2.42]-[2.43].

In the power flow control, FACTS controllers based on AC-link converters have been developed analogously to the DC-link based FACTS controllers. Similarly to the SSSC, the *Xi controller* is proposed as a controllable capacitive reactance [2.44], Fig 2.8. Switches S1 and S2, in Fig 2.8, operate under the same switching function in a complementary way. The operational principle can be divided in two states: when capacitors are connected to the system through a series injection transformer, S_1 *on*, and when the series injection transformer is shorted and the primary winding exhibits low impedance, S_2 *on*.

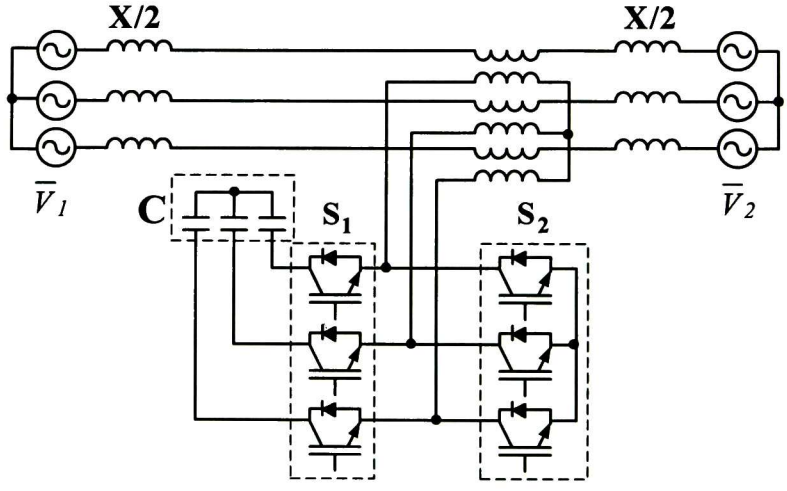

Figure 2.8. AC-link converter based series compensator (Xi controller).

Analogously to the unified power flow controller "UPFC", advanced controllers are developed such as the *Gamma controller*, which can control independently the active and reactive power on transmission line [2.36]-[2.37], Fig. 2.9. Gamma controller is constituted by a set of phase shift transformers that generates N three-phase voltages with a phase shift of $2\pi/N$ between them. The set produces four three-phase voltages shifted 90 electrical degrees between them. By PWM, a 4x1 vector switching converter can synthesize a three-phase voltage with controlled amplitude and phase. Injecting the generated voltage in series with a transmission line, the active and reactive power flow can be controlled in an independent way.

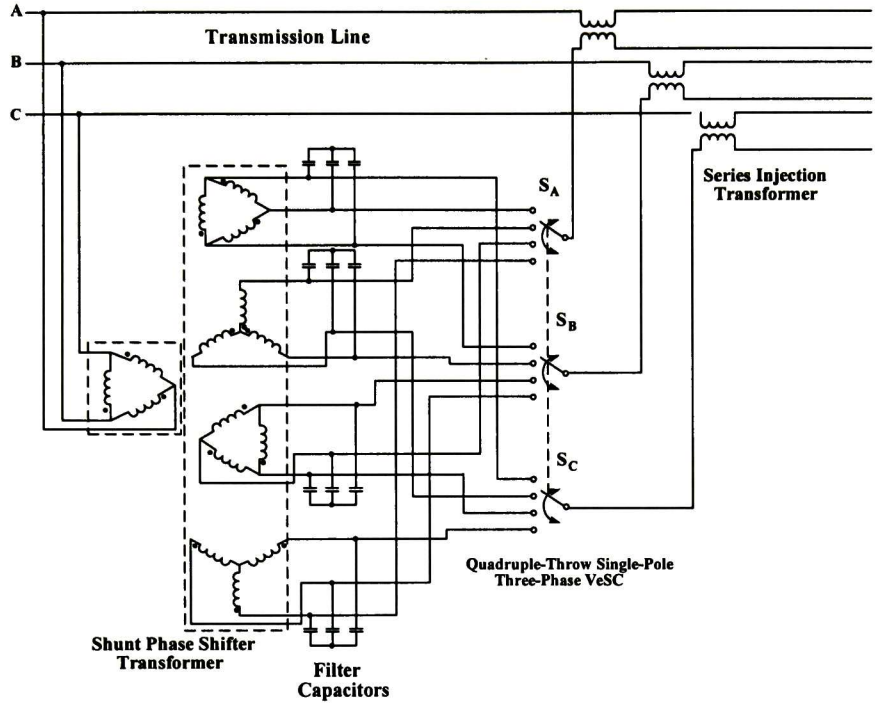

Figure 2.9. Gamma Controller

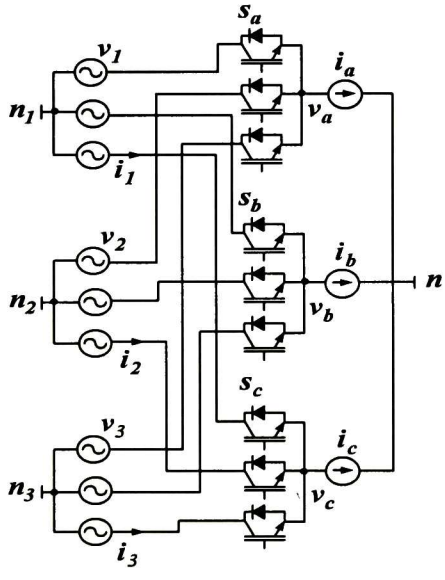

Figure 2.10. 3X1 Vector switching converter

FACTS controllers recently proposed work under the Vector Switching Converter (VeSC) principle [2.36]. The VeSC couples several three-phase voltage sources with several three-phase current sources in complex interconnections [2.45], Fig. 2.10. The systems' buses are considered voltage sources while loads and series injection transformers are current sources. Series inductor or shunt capacitors can be added to modify voltage or current sources into current or voltage sources respectively, then systems' buses can be coupled as current sources using series inductors.

2.5 Conclusions

In this chapter, the main power quality issues have been briefly reviewed. It was known from various power quality researches that most of power quality problems are related to voltage sags, swells, imbalance and harmonic distortion, and they can cause serious power distribution problems which can result in millionaire losses. A summary of the-state-of-the art methods proposed for voltage compensation has been presented along with the actual tendencies. It has been shown that many kinds of methods can be used for the purpose of this research, and the AC-AC conversion technology has been successfully used in DVR topologies for sag mitigation and in FACTS devices with power flow control purposes. These various schemes for compensation have been reviewed to determine the direction of the research.

It is known that the DVR devices represent the best option concerning voltage compensation but recently conventional DC-link-based topologies have been replaced by novel AC-link topologies due to the advantages offered by this new technology. Among the existing AC-AC converter configurations, the set of matrix converters' operating features is a quite attractive choice to substitute the DC-link configuration in conventional controller devices.

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CHAPTER III

Fundamentals of the Matrix Converter Technology

This chapter is an introductory material to the matrix converter technology. It presents the state-of-the-art in the matrix converter technology. First, a historical overview is presented, departing from the former static frequency changers until the actual matrix converter configuration. Then, the most significant technological aspects concerning the performance of the converter are reviewed, emphasizing issues that have to be taken into account for practical implementation. Since this converter employs bidirectional switches, a specific bidirectional switch commutation technique is presented. Finally, different modulation strategies applied to device are summarized.

3.1 Background

Documented history about static direct frequency changer begins in 1923 with L. A. Hazeltine's work [3.1], in which the fundamental principle for synthesizing an AC voltage waveform of controllable frequency from a multi-phase AC voltage supply of known frequency was stated. However, his system could not be implemented because electric valves with appropriate characteristics and capacity were unavailable [3.2].

During the 30's, practical experimental results were published through mercury arc valves available at the time [3.3]-[3.4]. In the results presented, variable output frequencies below input levels as well as variable output voltage magnitude were accomplish by means of controlling switching angles in the valves. Based on these valves, the term cycle-converter was introduced by H. Rissik [3.5]-[3.6].

At the end of 50's, the evolution of the silicon controlled rectifier (SCR) or thyristor, along with advantages offered over mercury arc rectifiers, such as higher commutation speed,

lower voltage fall in *on-state,* compact and robust construction, etc., aroused the motivation of researchers over applications concerning power systems with constant output frequency – variable speed [3.7]-[3.12].

In the mid 60's, some researchers had achieved important progress towards overcome obstacles associated to waveform distortion in frequency changers [3.13]-[3.14]. In spite of the inherent limitation of thyristors about turn-off just by natural commutation, some researchers aware of cycloconverters potential, persevere on develop a technology based on on-line commutation and succeeded in terms of output voltage amplitude and frequency control. The main field of application was in AC electric motors, fulfilling the industrial requirements imposed for DC motors. Cycloconverters became the perfect choice for controlling large AC motors spinning at low speed [3.15]-[3.27].

It was until power electronic devices with turn-off capability were developed for high power capacity, at the end of 70's, that static frequency changers expand to new capabilities such as input power factor control [3.28]-[3.30], and novel topologies for power conversion appeared [3.31]-[3.32]. Two theoretical publications by L. Gyugyi and B. R. Pelly [3.33]-[3.34] enclose an analysis of different types of frequency changers terminal characteristics including a complete study about the natural commutated cycle-converter (NCC). This work was followed by other publications by W. McMurray [3.35], covering theory and design of cycloconverters. In 1976, L. Gyugyi and B. R. Pelly published "Static power frequency changers" [3.2]. The authors summarize the available knowledge in the field of static frequency changers at the time, in a mathematical frame and state the future trends for the development of frequency changers based on forced commutation. The book became the main reference of that period. Since then, evolution of frequency changers has been taking place due to advances in semiconductor technology, developing of novel topologies and the incursion of new modulation and control techniques.

The real developing of matrix converter starts with two publications by M. Venturini and A. Alesina [3.36]-[3.37] in 1980. In these works a novel frequency changer was proposed, able to operate with input/output sinusoidal signals, bidirectional power transfer, controllable power factor and reactive power generation. One of their main contributions is the mathematical analysis that describes the behavior of converter for low frequency operation. This modulation technique is also known as direct transference function. Additionally, the use of matrix converters (term adopted for static frequency changers whose topology consists on a matrix of bidirectional power switches) was proposed for AC-AC, DC-AC and DC-DC types of conversion, with a buck or boost.

In the first control algorithm presented by Venturini [3.37], the input current waveform was distorted, there was not power factor control and the maximum input/output achieved voltage magnitude relation was 50 percent. A second Venturini's control strategy presented

several advantages over the first one, such as: limited input power factor control [3.38]-[3.39], better input current quality [3.40] and a maximum of 86.6 percent in voltage magnitude relationship [3.41]-[3.42]. The really controllable input power factor was obtained by Asher, through novel control algorithms [3.43], based on the combination of input and output phase displacements.

Among the different types of control algorithms developed for matrix converter operation, there are some identified as scalar techniques [3.44]-[3.47], which demand a lot of mathematical calculations. In 1983, Rodríguez introduced a conceptually different control technique based on the idea of the presence of a hypothetic DC-link [3.48], modulation also known as indirect transfer function. In 1985-86 Ziogas gives a mathematical formalization to Rodríguez's idea in [3.49]. Likewise in [3.50]-[3.51], the use of Park's transformation in matrix converter analysis and control was introduced. A series of publications made by Huber [3.52]-[3.54] present the space vector modulation (SVM) concept applied to matrix converter control and, along with Borojevic, establish a model for direct AC-AC converter. By applying the SVM strategies to matrix converter it is possible to accomplish the maximum theoretical ratio between input/output voltages, a high quality input current and a controllable input power factor by reducing the mathematical calculations.

In 1992, D. G. Colmes and T. A. Lipo applied the AC-AC converters theory to controllable inverters and rectifiers [3.55]-[3.56], in order to integrate different applications in one system. In this manner, a one-phase to three-phase matrix converters can operate in every possible configuration, that is, AC-AC, AC-DC, DC-AC and DC-DC. To change from one specific application to another just some software modifications have to be taking into account.

In spite of all the theoretical background, there is still a lot of work to do in matrix converter technology maturation process towards industrial implementation.

3.2 Introduction to Matrix Converter Technology

A matrix converter consists of nine bidirectional switches, arranged in three groups of three, each group being associated with an output line. This arrangement of bidirectional switches connects any of the input lines *a*, *b*, or *c* to any of the output lines *A*, *B*, or *C*, Fig 3.1. A bidirectional switch is able to control the current and to block the voltage in both directions. If the input and the output three-phase systems are orthogonal disposed, the converter diagram becomes similar to a matrix, with the rows consisting of the three input lines (*a*, *b*, *c*), the columns consisting of the three output lines (*A*, *B*, *C*) and bidirectional switches connecting each row to each column. There are two basic rules that ensure matrix converter proper and safe operation:

- Do not connect two different input lines to the same output line (short-circuit of the mains, which causes over-currents);
- Do not disconnect the output line circuits (interrupt inductive loads, which causes over-voltages).

Therefore, an output line has to be all the time connected to a single input line. By following the basic rules mentioned before, the maximum number of permitted switching states of the matrix converter is reduced from 512 to 27, as it is shown in Appendix A.

A matrix with existential functions M_{ij} representing the state of each bi-directional power switch, where $M_{ij} = 0$ for *off-state* and $M_{ij} = 1$ for *on-state*, can be used to represent the matrix output voltages (v_A, v_B, v_C) as functions of the input voltages (v_a, v_b, v_c) as follows,

$$\begin{bmatrix} v_{AB} \\ v_{BC} \\ v_{CA} \end{bmatrix} = \begin{bmatrix} M_{11} & M_{12} & M_{13} \\ M_{21} & T_{22} & T_{23} \\ M_{31} & M_{32} & M_{33} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \text{ or } \mathbf{V}_{ol} = \mathbf{M} \times \mathbf{V}_{inp} \tag{3.1}$$

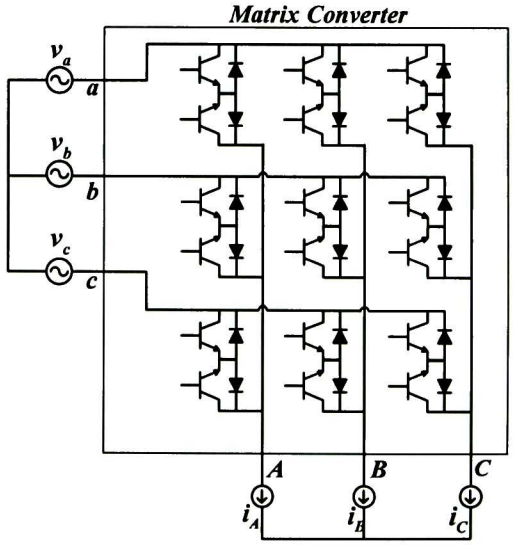

Figure 3.1. Basic matrix converter structure

Due to the instantaneous power transfer of the matrix converter, the electrical parameters (voltage, current) in one side may be reconstructed from the corresponding parameters in the other side, at any instant. The output currents are a result of applying the previously determined output voltages to a given load. Input/output currents relationship can be expressed by:

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} M_{11} & M_{21} & M_{31} \\ M_{12} & M_{22} & M_{32} \\ M_{13} & M_{23} & M_{33} \end{bmatrix} \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} \text{ or } \mathbf{I}_{in} = \mathbf{M}^T \times \mathbf{I}_{out} \tag{3.2}$$

where $\mathbf{M}^T$ is the transpose matrix of **M**.

Due to the lack of energy storage devices the output voltage is generated directly from the input voltages, so if not restrictions are imposed to output frequency, the maximum line-to-line voltage in a three-phase to three-phase converter will be the corresponding to the minimum value of input voltage enveloping. It is analogous to a voltage generated by an inverter fed by the rectified input voltage through a non-controlled bridge rectifier. Thus the maximum output voltage achieved by any commutation strategy applied to matrix converter will be equal to 0.866.

This restriction, inherent to the direct converter itself, is its most important drawback as it limits its operation in standard AC motors. Nonetheless, it is not a problem for other applications such as voltage compensation devices.

Another relevant aspect concerning output voltages and input currents is the harmonic content. The line-to-line output voltage is made up by the three input voltages, reducing the magnitude of harmonics around switching frequency compared to a voltage source inverter (VSI), as it is shown in [3.57]. Likewise, in [3.57] a comparison of the input current THD for an AC-AC indirect converter (non-controllable rectifier-inverter configuration) and a matrix converter, is also presented. It can be seen on the publication, how the input filter in the matrix converter reduces the THD to a 4% approximately compared to a THD of near 39% generated by the indirect converter.

3.3 Analysis of Bidirectional Power Switches

The direct AC-AC converter requires the presence of bidirectional power switches able to conduct the current and to block voltages in both directions. Unfortunately those kinds of devices are not available yet in the market (at least for high power performance). In [3.58] a new power device for matrix converter applications is proposed: the reverse blocking IGBT (RIGBT), decreasing the number of devices per phase. This will create conditions to increase reliability and efficiency of the matrix converter because conduction losses will be produced only by a single RIGBT.

Meanwhile a true force-commutated bidirectional switch is industrially produced; the solution is to implement bidirectional switches with discrete components such as IGBT or

MOSFET devices. Using unidirectional devices available on the market, there are five ways to obtain a bidirectional switch:

- Diode embedded switch (Fig 3.2a). This commutation cell requires only one gate driver and one active switch. It has higher conduction losses because the current path consists of two FRDs and one IGBT and current direction can be controlled so all commutations have to be hard switched.

- Common emitter switches (Fig 3.2b). This cell is built up by two FRDs and two IGBTs connected in anti-parallel. FRDs incorporate inverse blocking capability. In this arrangement conduction losses are low because the current path consist only of one FRD and one IGBT and current direction control can be accomplish for soft switching implementation.

- Common collector switches (Fig 3.2c). In this topology conduction losses are the same as for common emitter switch, but only six isolated voltage sources are required for the drivers.

- Bidirectional topologies using CSC switches which can drain voltage in only one direction (Fig 3.2d-e). Connecting these cells in anti-parallel, both current directions can be drain while blocking voltage in both polarities.

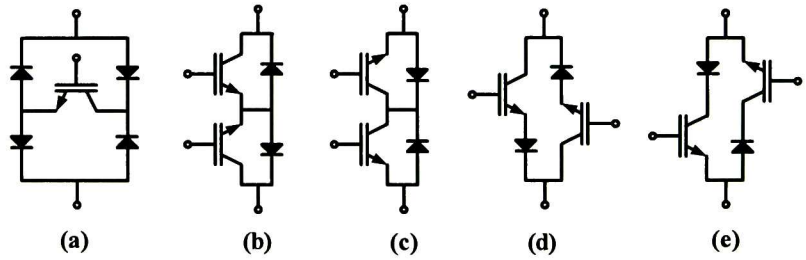

Figure 3.2. Bidirectional switch topologies using unidirectional components

Although it is possible to achieve bidirectional switches from combining unidirectional components, some attempts have been reported in literature [3.59], as a trend to incorporate complex silicon structures in power modules. This type of power modules has remarkable advantage of reducing stray inductances in current commutation paths.

3.4 Current Commutation Techniques

A safe current commutation between two bidirectional power cells in a matrix converter is not a simple process to achieve as in a VSI, because in the matrix there is not a natural path for current flow. Thus, in matrix converter operation, time of switching signals sent to

bidirectional power cells is very critical. Inaccurate or delayed signals on the gate drivers and the non-instantaneous switching of the bidirectional power cells can provoke over-currents by short-circuiting the input voltage source terminals and over-voltages due to inductive load currents' interruptions [3.60]-[3.61].

There are two options to eliminate the risk of shoot-through in matrix converters. Some researches employs snubber circuits [3.62],which results in complicated arrangements and increasing of losses; while others implement specific commutation techniques by operating the bidirectional switches [3.63]-[3.65]. The commutation technique depends on the type of bidirectional switches employed in the matrix converter hardware.

The two basic methods to perform the commutation in bidirectional cells are:

- The dead-time current commutation, referred as "break before made" is shown in Fig 3.3c. In this method, there is a time interval where none of the power cells is shot *on*. By using dead-times the load is momentarily disconnected. As consequence this technique causes high switching losses and a clamp circuit or snubber circuits connected to the output to provide continuity of the load current is necessary.

- The overlap current commutation, referred as "make before break" is shown in Fig 3.3d. This method consists in turning on the on-coming switch while the off-going switch is still conducting, to provide continuity for the output line circuit. This will cause high circulating currents between input phases, and makes it necessary to add extra chokes to limit these currents.

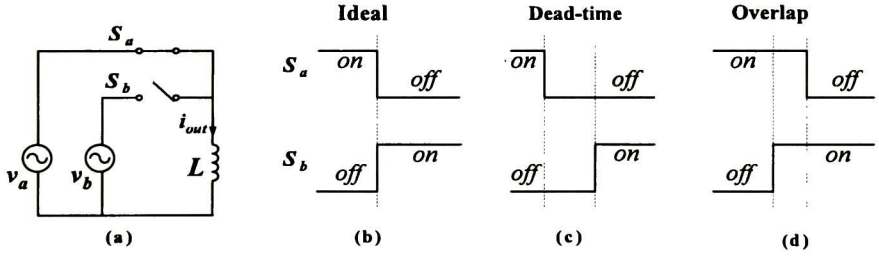

Figure 3.3. Commutation of the out phase from input phase *a* to input phase *b*: a) Power circuit; b) Ideal commutation; c) Dead-time commutation; d) Overlap commutation.

Both methods require extra reactive elements and produce high losses. A reliable method for current commutation is the strategy known as four step commutation technique. Basically, both IGBTs are shot active allowing current flow in both directions. For implementing this strategy is necessary the use of bidirectional cells with anti-paralleled unidirectional switches, which provide independent control for each direction of the current. Thus, depending on the direction of the output current or on the magnitude of the

input voltages involved in the commutation process, the first action is to disable the current path for circulating currents and the second is to apply overlapping for the on-coming switch with the off-going switch. Therefore the risk of short circuit on the input side is eliminated, and semi-soft commutation, is achieved.

3.4.1 Four step commutation strategy

This commutation strategy takes place in four steps. For a better comprehension, the circuit shown in Fig. 3.4 is analyzed.

- Step one: The non-conducting switch (S_{1p}) is turned *off*, Fig 3.4b. This way, current direction is not able to change sign.

- Step two: The switch that would conduct the current (S_{2n}) is turned *on*, Fig 3.4c. Now, there is unidirectional connection between input lines, but no circulating current may occur, since S_{1n} and S_{2p} are *off*.

- Step three: The switch S_{1p} is turned *off*, Fig 3.4d. At this time the current is forced to switch from input phase *1* to input phase *2*.

- Step four: The non-conducting switch (S_{2n}) is turned *on*, Fig 3.4e. This is a passive step, with the purpose to re-establish the four quadrant characteristic of the AC switch, so the currents can change sign naturally.

As mentioned above, the current direction is required for implementing this method, which makes the current direction measurement necessary. Fig. 3.4 displays the possible path for the output current allowed by the four step commutation strategy for both current signs.

When implementing this strategy, the duration of commutation steps is one important aspect to be considered. The duration of the passive commutation steps (1 and 4) is non critical, because the switch on the bidirectional cell that do not change state allows the current flow; then, the complementary switch does not have to change so fast. Duration of the active commutations (2 and 3) is critical and should be chosen in agreement with the switching characteristics of the devices employed.

Other problems that can adversely affect the matrix converter operation by employing multistep commutation techniques are related to errors on the current sign caused by commutation near to zero output current and the current sign detection method utilized. Current transducers based on Hall Effect are commonly used in order to control properly the commutation, but methods based on the voltage drop across unidirectional switches have been also proposed.

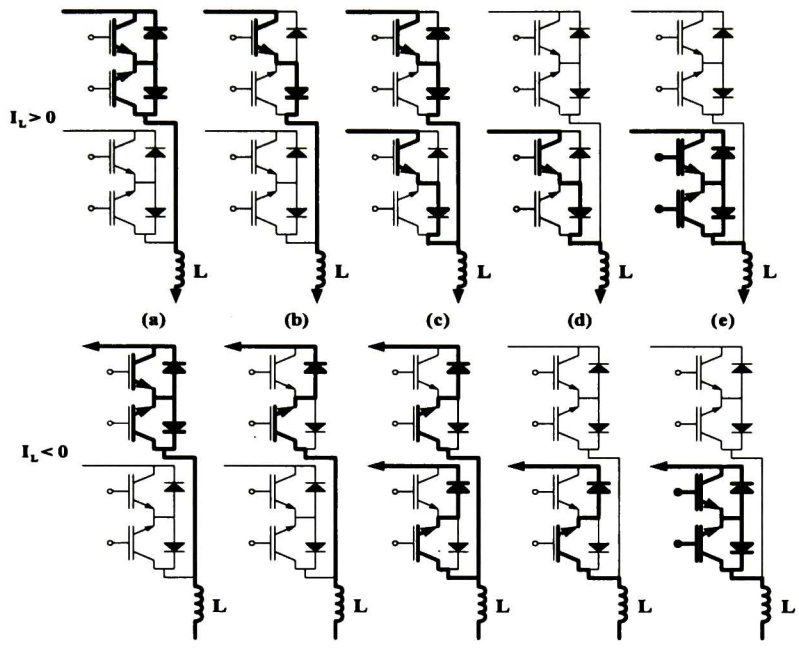

Figure 3.4. Path current allowed during the four-step commutation

3.5 Modulation Techniques

Output-voltage in a direct AC-AC converter is integrated by portions of each one of the input-voltage phases in sequences and time intervals well defined. Likewise, input currents are made up by portions of the output-currents. A typical switching pattern is exhibited in Fig 3.5.

Considering a high switching frequency applied to the bidirectional power switches, an output-voltage with controllable amplitude and low variable frequency can be generated through the modulation of duty cycles $m_{ij}(t)$. Where $m_{ij}(t)$ is the duty cycle for the power switch M_{ij} defined as:

$$m_{ij}(t) = \frac{t_{ij}}{T_s} \tag{3.3}$$

where t_{ij} is the time elapsed while switch M_{ij} is *on* during the commutation period T_s. Duty cycle can only have the next values:

$$0 < m_{ij}(t) < 1 \qquad i = \{1,2,3\} \quad j = \{1,2,3\}, \ \forall t \tag{3.4}$$

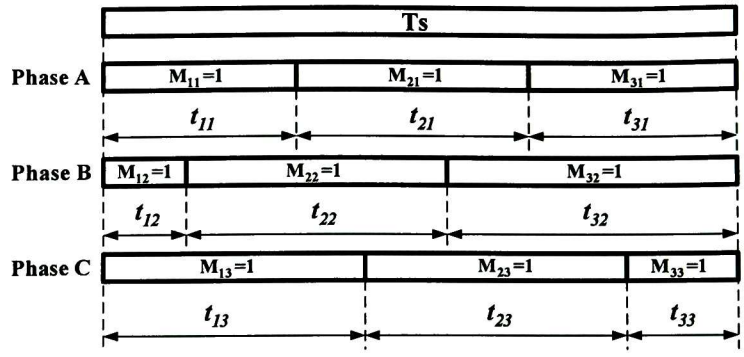

Figure 3.5. Typical switching pattern

Low frequency transference matrix can be stated as:

$$\mathbf{M}(t)=\begin{bmatrix} m_{11}(t) & m_{12}(t) & m_{13}(t) \\ m_{21}(t) & m_{22}(t) & m_{23}(t) \\ m_{31}(t) & m_{32}(t) & m_{33}(t) \end{bmatrix} \tag{3.5}$$

This matrix can be used to define the low frequency component of output voltage, given by:

$$\begin{bmatrix} v_A(t) \\ v_B(t) \\ v_C(t) \end{bmatrix} = \begin{bmatrix} m_{11}(t) & m_{12}(t) & m_{13}(t) \\ m_{21}(t) & m_{22}(t) & m_{23}(t) \\ m_{31}(t) & m_{32}(t) & m_{33}(t) \end{bmatrix} \begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} \text{ or } \mathbf{V}_{outp} = \mathbf{M}(t)\mathbf{x}\mathbf{V}_{inp} \tag{3.6}$$

Low frequency input-current component is,

$$\begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix} = \begin{bmatrix} m_{11}(t) & m_{21}(t) & m_{31}(t) \\ m_{12}(t) & m_{22}(t) & m_{32}(t) \\ m_{13}(t) & m_{23}(t) & m_{33}(t) \end{bmatrix} \begin{bmatrix} i_A(t) \\ i_B(t) \\ i_C(t) \end{bmatrix} \text{ or } \mathbf{I}_{in} = \mathbf{M}(t)^T \mathbf{x}\mathbf{I}_{out} \tag{3.7}$$

Where in order to fulfill the basic commutation rules for matrix converters,

$$\sum_{i=1,2,3} m_{1i}(t) = \sum_{i=1,2,3} m_{2i}(t) = \sum_{i=1,2,3} m_{3i}(t) \tag{3.8}$$

The matrix converter control's main problem may be stated as: "*For a given set of input-voltages and output currents, a modulation matrix M(t) able to accomplish a set of dependant output-voltages and input-currents, is required*"

As was reviewed in the initial section, the first modulator proposed for matrix converter was made by M. Venturini and A. Alesina, using a complicated scalar model [3.36]-[3.37]. After that, some algorithms based on the Venturini modulation were proposed, known as scalar techniques. Next, the indirect modulation was introduced. This approach simplified the modulator model by making possible to implement classical PWM modulation strategies in matrix converters. Modulation models using SVM permits control the converter even under unbalanced and distorted conditions. In the next sections, these common modulation techniques are briefly presented.

3.5.1 Scalar algorihtms

In this kind of algorithms the magnitude of a voltage signal, denoted as Venturini modulation method establish independent relations for each output, by sampling and distributing portions of input voltages in such a way that the average result follows the reference output phase voltage. Assuming that the input voltages are given by:

$$\overline{V}_{in} = V_{in} \cdot \begin{bmatrix} \cos(\omega_{in} t) \\ \cos\left(\omega_{in} t + \frac{2\pi}{3}\right) \\ \cos\left(\omega_{in} t + \frac{4\pi}{3}\right) \end{bmatrix} \tag{3.9}$$

and the currents can be expressed as,

$$\overline{I}_{out} = I_o \cdot \begin{bmatrix} \cos(\omega_{out} t + \theta_{out}) \\ \cos\left(\omega_{out} t + \frac{2\pi}{3} + \theta_{out}\right) \\ \cos\left(\omega_{out} t + \frac{4\pi}{3} + \theta_{out}\right) \end{bmatrix} \tag{3.10}$$

The desired input-current and output-voltage vectors can be denoted by:

$$\overline{V}_{out} = q \cdot V_{in} \cdot \begin{bmatrix} \cos(\omega_{out} t) \\ \cos\left(\omega_{out} t + \frac{2\pi}{3}\right) \\ \cos\left(\omega_{out} t + \frac{4\pi}{3}\right) \end{bmatrix} \tag{3.11}$$

$$\bar{I}_{out} = q \cdot I_o \cdot \begin{bmatrix} \cos(\omega_{in}t + \theta_{in}) \\ \cos\left(\omega_{in}t + \frac{2\pi}{3} + \theta_{in}\right) \\ \cos\left(\omega_{in}t + \frac{4\pi}{3} + \theta_{in}\right) \end{bmatrix} \tag{3.12}$$

where q is the matrix converter voltage gain.

The two solutions for the conversion matrix, proposed by Venturini are,

$$M_1(t) = \frac{1}{3} \cdot \begin{bmatrix} 1+2q\cos(\omega_m t) & 1+2q\cos(\omega_m t - \frac{2\pi}{3}) & 1+2q\cos(\omega_m t - \frac{4\pi}{3}) \\ 1+2q\cos(\omega_m t - \frac{4\pi}{3}) & 1+2q\cos(\omega_m t) & 1+2q\cos(\omega_m t - \frac{2\pi}{3}) \\ 1+2q\cos(\omega_m t - \frac{2\pi}{3}) & 1+2q\cos(\omega_m t - \frac{4\pi}{3}) & 1+2q\cos(\omega_m t) \end{bmatrix} \tag{3.13}$$

where $\omega_m = (\omega_{out} - \omega_{in})$

$$M_2(t) = \frac{1}{3} \cdot \begin{bmatrix} 1+2q\cos(\omega_m t) & 1+2q\cos(\omega_m t - \frac{2\pi}{3}) & 1+2q\cos(\omega_m t - \frac{4\pi}{3}) \\ 1+2q\cos(\omega_m t - \frac{2\pi}{3}) & 1+2q\cos(\omega_m t - \frac{4\pi}{3}) & 1+2q\cos(\omega_m t) \\ 1+2q\cos(\omega_m t - \frac{4\pi}{3}) & 1+2q\cos(\omega_m t) & 1+2q\cos(\omega_m t - \frac{2\pi}{3}) \end{bmatrix} \tag{3.14}$$

where $\omega_m = -(\omega_{out} + \omega_{in})$

$M_1(t)$ establish that $\theta_{in} = \theta_{out}$, while $M_2(t)$ states that $\theta_{in} = -\theta_{out}$. Combining both solutions power factor control can be achieved.

$$\mathbf{M}(t) = \alpha_1 \cdot \mathbf{M}_1(t) + \alpha_2 \cdot \mathbf{M}_2(t) \tag{3.15}$$

where $\alpha_1 + \alpha_2 = 1$, and for $\alpha_1 = \alpha_2$ the matrix converter input power factor is unitary.

Even when this solution allows input power factor control, its main drawback resides in its limited (50 %) input/output voltage ratio as is represented in Fig 3.6.

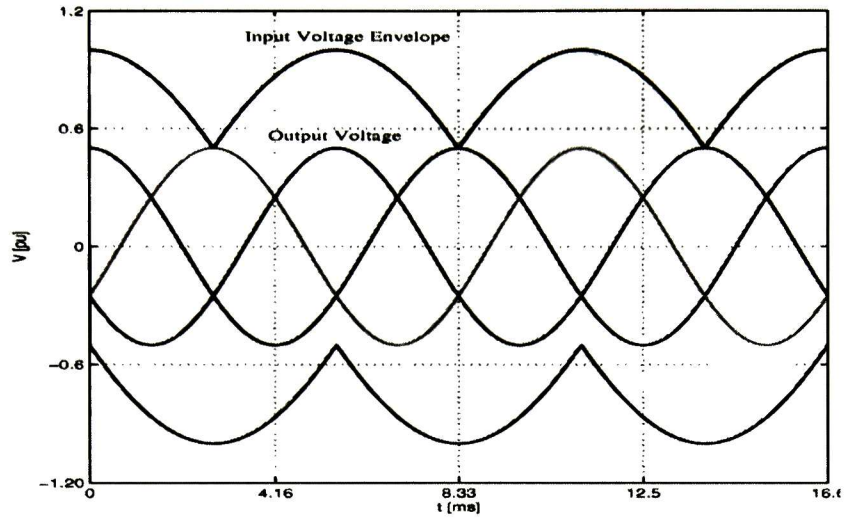

Figure 3.6. Output voltage limited to 50%

In order to provide maximum voltage transfer ratio, injection of third harmonics on the output voltage is needed. Then, the reference output voltage becomes,

$$\overline{V}_{out} = q \cdot \overline{V}_{in} \begin{bmatrix} \cos(\omega_{out}t) - \frac{1}{6}\cos(3\omega_{out}t) + \frac{1}{2\sqrt{3}}\cos(3\omega_{in}t) \\ \cos(\omega_{out}t + \frac{2\pi}{3}) - \frac{1}{6}\cos(3\omega_{out}t) + \frac{1}{2\sqrt{3}}\cos(3\omega_{in}t) \\ \cos(\omega_{out}t + \frac{4\pi}{3}) - \frac{1}{6}\cos(3\omega_{out}t) + \frac{1}{2\sqrt{3}}\cos(3\omega_{in}t) \end{bmatrix} \tag{3.11}$$

Fig 3.7 illustrates this strategy. Therefore duty cycles are given by,

$$m_{ij} = \frac{t_{ij}}{T_s} = \frac{1}{3}\left[1 + \frac{2v_i(t)\cdot v_j(t)}{V_{in}^2} + \frac{4q}{3\sqrt{3}}\sin(\omega_{in}t + \beta_i)\sin(3\omega_{in}t)\right] \tag{3.12}$$

where
- $i = \{(1,A),(2,B),(3,C)\}$ $j = \{(1,a),(2,b),(3,c)\}$
- $\beta_i = \{0, \frac{2\pi}{3}, \frac{4\pi}{3}\}$ para $i = \{1,2,3\}$
- $v_j(t)$ includes third harmonics addition
- V_{in} is the RMS value of input voltage system

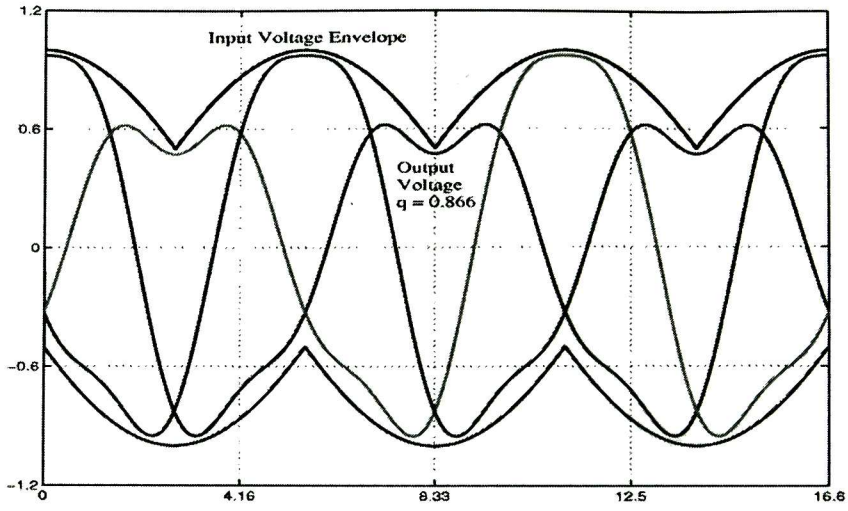

Figure 3.7. Maximum output voltage (86.6%)

This algorithm requires complex mathematical calculations for duty-cycles estimation, which represents time consuming computations, besides it requires nine commutations in the switching period because both type of vectors, rotating and active, are inherent generated. Other modulator models have been derived employing only one type of switching state vectors, which simplified the mathematical models. In [3.66] only rotating vectors of both, direct ad inverse sequence, are used, in conjunction with zero vectors in order to vary smoothly the amplitude and the instantaneous frequency of the output voltage.

3.5.2 Indirect modulation

In the Indirect Space Modulation Method (ISVM) [3.68], the modulation process is split into two steps as indicated in (3.13)

$$\overline{V}_{out} = \left(\mathbf{A}\overline{V}_{in}\right)\mathbf{B} \tag{3.13}$$

where $\overline{V}_{in}$ is defined by (3.9).

In (3.13), pre multiplication of the input voltages by A generates a fictitious DC-link, while post multiplication by B generates the desired output by modulating the fictitious DC-link inverter transformation due to the similarity with the conventional rectifier/DC-link/inverter system. A is generally referred to as the rectifier transformation, and B as the inverter transformation due to the similarity with a traditional rectifier/DC-link/inverter system. A is given by,

$$\mathbf{A} = K_A \begin{bmatrix} \cos(\omega_{in}t) \\ \cos(\omega_{in}t + 2\pi/3) \\ \cos(\omega_{in}t + 4\pi/3) \end{bmatrix}^T \tag{3.14}$$

Hence,

$$\mathbf{A}\overline{V}_{in} = K_A V_{in} \begin{bmatrix} \cos(\omega_{in}t) \\ \cos(\omega_{in}t + 2\pi/3) \\ \cos(\omega_{in}t + 4\pi/3) \end{bmatrix}^T \begin{bmatrix} \cos(\omega_{in}t) \\ \cos(\omega_{in}t + 2\pi/3) \\ \cos(\omega_{in}t + 4\pi/3) \end{bmatrix} = \frac{3K_A V_{in}}{2} \tag{3.15}$$

B is defined as,

$$\mathbf{B} = K_B \begin{bmatrix} \cos(\omega_{out}t) \\ \cos(\omega_{out}t + 2\pi/3) \\ \cos(\omega_{out}t + 4\pi/3) \end{bmatrix} \tag{3.16}$$

Hence,

$$\overline{V}_{out} = (\mathbf{A}\overline{V}_{in})\mathbf{B} = \frac{3K_A K_B V_{in}}{2} \begin{bmatrix} \cos(\omega_{out}t) \\ \cos(\omega_{out}t + 2\pi/3) \\ \cos(\omega_{out}t + 4\pi/3) \end{bmatrix} \tag{3.17}$$

Voltage ratio $q = 3K_AK_B/2$. A and B are not continuous in time but must be implemented by a suitable choice of the switching states.

The voltage ratio obtainable is greater than the one obtained with other methods but improvement is only obtained at the expense of the quality of the input currents, the output voltages or both. For voltages of $q > 0.866$, the mean output voltage no longer equals the target output voltage in each switching interval, this inevitably leads to low frequency distortion in output voltage and/or the input current compared to other methods with $q < 0.866$. For $q < 0.866$, the indirect method yields very similar results to the direct methods.

3.5.3 Space vector modulation methods

An effective way to generate the desired PWM pattern is to use the space vector modulation techniques. Space vector modulation technique uses a combination of the two adjacent vectors and a zero-vector to produce the reference vector. The proportion between

the two adjacent vectors gives the direction and the zero-vector duty cycle determines the magnitude of the reference vector. The input current vector $\overline{I}_{in}$ and the output voltage vector $\overline{U}_{outl}$ are the reference vectors. In order to implement the DSVM, it is necessary to determine the position of the two reference vectors. The input reference current vector $\overline{I}_{in}$ is given by the input voltage vector $\overline{U}_{inp}$ in case instantaneous unitary power factor is desired, or is given by a custom strategy to compensate for unbalanced and distorted input voltage system [3.67]. The output reference voltage vector $\overline{U}_{outl}$ results of a vector control scheme. Vector modulation strategies allow:

- Output frequency control
- Output voltage magnitude and phase control
- Input current phase control, which means input power factor control

A variant of the Direct Space Vector Modulation (DSVM) is explained in detail in Chapter IV. Another approach based on space vector modulation technique is modeling the direct AC-AC converter as the combination of an AC-DC converter and a DC-AC converter. In this way, the matrix converter can be controlled indirectly through the rectifier and inverter controls. This technique is known as Indirect Space Vector Modulation (ISVM) [3.52]-[3.54].

As sated before, space vector modulation techniques are based on Park's reference vectors tracking [3.57], Fig 3.8.

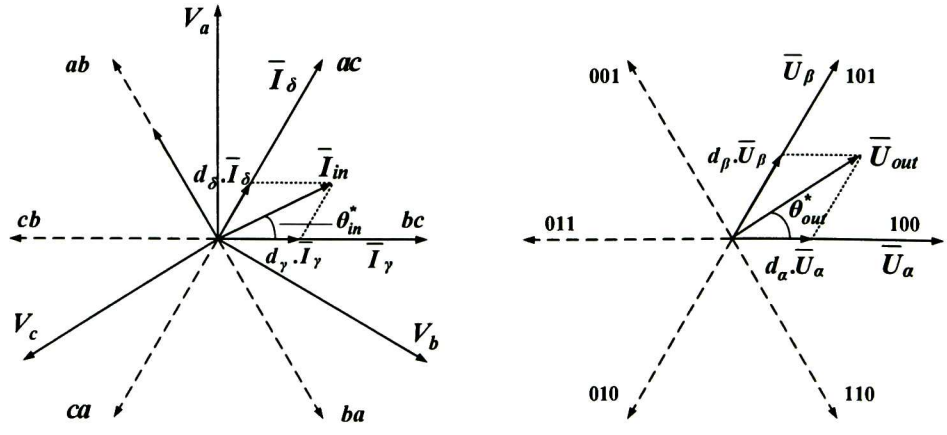

Figure 3.8. Reference vector tracking

Duty cycles of the active switching vectors are calculated for the rectification stage by using,

$$d_\gamma = m_I \cdot \sin\left(\frac{\pi}{3} - \theta^*_{in}\right) \tag{3.18}$$

$$d_\delta = m_I \cdot \sin\left(\theta^*_{in}\right) \tag{3.19}$$

For the inversion stage,

$$d_\alpha = m_U \cdot \sin\left(\frac{\pi}{3} - \theta^*_{out}\right) \tag{3.20}$$

$$d_\beta = m_U \cdot \sin\left(\theta^*_{out}\right) \tag{3.21}$$

where m_I and m_U are the rectification and inversion stage modulation indexes, θ^*_{in} and θ^*_{out} are the angles within their respective sector of the input and output voltage reference vectors. Usually $m_I = 1$ and $m_U = U_{out}/U_{pn}$, in ideal sinusoidal and balance input voltages:

$$U_{pn} = d\gamma.U_{line-\gamma} + d_\delta.U_{line-\delta} = 0.86 \cdot \sqrt{2} \cdot U_{line} \tag{3.22}$$

To obtain a correct balance of the input currents and the output voltages, the modulation pattern should be a combination of all the rectification and inversion duty-cycles (αγ-αδ-βδ-βγ-0). The duty cycle of each sequence is determined as a product of the corresponding duty cycles:

$$d_{\alpha\gamma} = d_\alpha \cdot d\gamma;\ d_{\alpha\delta} = d_\alpha \cdot d_\delta;\ d_{\beta\delta} = d_\beta \cdot d_\delta;\ d_{\beta\gamma} = d_\beta \cdot d\gamma \tag{3.23}$$

Therefore, duration of the zero vector can be calculated by

$$d_0 = 1 - \left(d_{\alpha\gamma} + d_{\alpha\delta} + d_{\beta\gamma} + d_{\beta\gamma}\right) \tag{3.24}$$

Finally, the duration of each sequence is calculated by multiplying the corresponding duty cycle times the switching period.

3.6 Overvoltage Protection Circuit

Matrix converter topology needs to be protected against overvoltage and over-current. Furthermore, due to the lack of an energy storage element this topology is more sensitive to disturbances and therefore more susceptible to failures. Disturbances, which may cause hardware failures, are:

- Faulty inter-switch commutations, as internal short-circuit of the mains or discontinuing the circuit of the motor currents;
- Shutdown of the matrix converter during an over-current situation, in the load side
- Possible overvoltage on the input side caused by the converter power-up or by voltage sags.

Protection issues of matrix converters have always commanded attention, in order to build a reliable prototype. A solution to solve some of the problems consists of connecting a clamp circuit on the output side [3.69], Fig. 3.9. The clamp circuit consists of two B6 fast recovery diode rectifiers back to back connected and a capacitor to store the energy accumulated in the leakage inductance of the load, caused by the output currents. The worst case regarding the energy level stored in the leakage inductance occurs when the output current reaches the over-current protection level, causing a converter shutdown.

Other interesting methods to lamp the reactive energy of the inductive load have been proposed. In [3.70] a new configuration using only six diodes is proposed. A strategy of protection against over-voltages employing varistors connected at the input and output terminals, plus an extra protection circuit for each IGBT is proposed in [3.71]

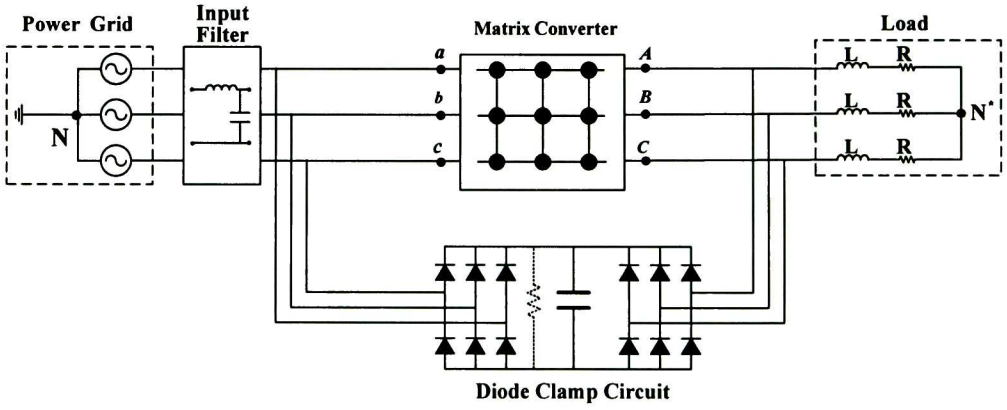

Figure 3.9. Diode Clamp circuit in matrix converter applications

3.7 Conclusions

This chapter has presented a compilation of around three decades of investigation concerning the direct ac-ac converter, since the first mathematical model to provide sine wave in – sine wave out operation was developed, to the actual situation of the matrix converter technology. It have been established the main components required for practical

implementation, as well as the protection issues and safe commutation techniques to ensure the proper operation.

The operational characteristics of the matrix converter, advantages and disadvantages, can be summarized as follows:

Advantages:

- It has not internal energy storage (DC-link)
- Theoretical unlimited output frequency
- Bidirectional power flow
- High quality output voltage
- High quality input current
- Controllable input power factor
- Four-quadrants operation
- Compact design
- Low level of acoustic noise when operates as driver of AC motors

Disadvantages:

- Low input/output voltage gain
- High number of solid state components
- Complex commutation scheme

Regarding the modulation strategies, some of them were briefly reviewed at the end of the chapter. In order to compare each strategy, several simulations were performed in the MATLAB software. Even when the results were not included in the chapter, they served to realize a comparison between the modulation techniques, from which the next statements can be mentioned:

- Scalar algorithms require more computational resources in order to perform the complex mathematical calculations required.
- The hardware requirements for implementation are the same in all algorithms, because all need to measure the same signals.
- Respect to the output voltages harmonic content, the vectorial strategies generates voltages with a harmonic spectrum slightly distorted. For low values in the voltage gain, q, the output voltages' distortion is important for all strategies.
- About the input current harmonic content, only differences are appreciated when the converter is operating with low values of q, being the vectorial techniques the ones with lower distortion.
- Finally, the input power factor control is simple and easy to implement in the vectorial strategies, in contrast with the scalar techniques.

In conclusion, for practical implementation the vectorial strategies are the best option. Among these two topologies, the direct SVM is more suitable to understand the operation of matrix converter because its analysis is based on the particularities of each switching configuration which reflects the output voltage vectors and input current vectors. As a result, the control of the output voltage reference can be derived directly by selecting the suitable switching patterns.

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CHAPTER IV

Modified DSVM Strategy

As it was stated in chapter III, three-phase matrix converters have advantages over traditional frequency changers such as four-quadrant operation capability, sinusoidal input/output waveforms, controllable input power factor and minimal energy storage requirements, etc. However, since the matrix converter performs direct power conversion and has no internal energy storage device, it is high sensitive to disturbances at the input port that are transmitted directly to the output side [4.1]. In order to speed up the maturation process of matrix converter technology towards industrial application, several performance and reliability issues of the matrix converter are being investigated, and the novel modulation strategies a particular case of interest [4.2].

In the present chapter a novel modulation technique denominated "Modified Direct Space Vector Modulation" is developed with the purpose of synthesize the reference output voltage vector despite the conditions presented in the input terminals of the matrix converter. The proposed alternative DSVM method has the advantage of easy implementation and improved power quality.

4.1 Introduction

The conventional modulation strategies are derived under the assumption that input voltages are sinusoidal and balanced, which results in ideal output waveforms. However, when unbalanced supply voltages are present, these strategies generate low-order harmonics in the input voltages [4.3]. With reference to the switching control methods proposed for deal with abnormal conditions at the input terminals, they are commonly based on two different approaches: the Venturini method as in [4.4], and the space vector modulation (SVM), [4.1],[4.3],[4.5]-[4.9]. In the algorithms proposed in [4.3], [4.5]-[4.8] the conversion process has been fictitiously divided in two stages: rectification and inversion, by introducing an imaginary DC-link. In [4.1],[4.9] a direct formulation of SVM is employed in order to analyze the input current performance of matrix converter. In [4.6], it has been shown that, it is possible to produce balanced and sinusoidal output voltages

even when the input voltages are unbalanced. In this case by taking into account the input/output power balance equation, it can be shown that non-sinusoidal input currents will appear. On the other hand, [4.9] deals with the performance evaluation of SVM controlled matrix converters under input and output unbalanced conditions. Finally, alternative control methods have been developed as in [4.10] were the authors were focused on minimizing the switching losses.

In applications concerning voltage compensation is a compelling requirement to generate a controllable output-voltage no matter the particular condition of the supplied voltages. In this chapter a modulation strategy based on the well known SVM algorithm is developed in order to synthesize controllable voltages in magnitude and waveform for compensation purposes, from unbalanced conditions and harmonic distortion in the supply voltages. The technique presented performs the power conversion directly from AC-to-AC and the calculation of the duty cycles relies on instantaneous samples of two of the three line-to-line input voltages. The final equations obtained are easy to implement in real time digital controllers.

4.2 Modified DSVM to Compensate Unbalanced and Distorted Input Voltages

The DSVM is presented in [4.11], considering a set of balanced input voltages. That technique is considered as a direct control strategy, since it is developed from the direct AC–AC converter model, different from those strategies developed from the AC-DC-AC model established by Huber and Borojevic [4.12]-[4.17].

Since one of the main objectives in this research is the implementation of a voltage compensator based on the matrix converter, to develop a modulation strategy that allows adequate converter operation under distorted conditions in the supply voltages is required.

4.2.1 Unbalanced conditions specification

In the SVM algorithm, the three phase framework is mapped into a complex vector in terms of $\alpha\beta$ coordinates, being the frequency translated on its speed of rotation and the amplitude on its modulus. The control strategy implies the modification of the amplitude and phase of the reference vector, from which the switches' triggering pulses are determined. Within the SVM technique the reference vector is time variant, thus it is possible accomplish studies at steady and transient regimes.

It is known that when the supply voltage is unbalanced and/or distorted, the matrix converter operation can be affected by the generation of output voltages and currents which are also unbalanced and distorted. To overcome such a shortcoming, is necessary to modify the duty cycles relations by incorporating the characteristics of the supply voltages into the computation. So as to develop a general strategy that encompasses typical abnormal input-voltage conditions is necessary to analyze the resulting space vectors. For unbalanced case, consider a three phase voltage system defined as follows,

$$\mathbf{V}_p = \begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} = \begin{bmatrix} V_{in}\sin(\omega t) \\ k_1 \cdot V_{in}\sin\left(\omega t - 2\pi/3 + \theta_1\right) \\ k_2 \cdot V_{in}\sin\left(\omega t + 2\pi/3 + \theta_2\right) \end{bmatrix} \tag{4.1}$$

where coefficients k_1 and k_2 specify the degree of unbalance in two of the input phase voltage magnitudes. Likewise, adding the angles θ_1 and θ_2, it is possible to admit angles different from $2\pi/3$ among phases. Under such conditions, the line-to-line input-voltages become:

$$\mathbf{V}_l = \begin{bmatrix} v_{ab}(t) \\ v_{bc}(t) \\ v_{ca}(t) \end{bmatrix} = \begin{bmatrix} x_1 \cdot V_{in}\sin\left(\omega t - \beta_1\right) \\ x_2 \cdot V_{in}\sin\left(\omega t + \beta_2\right) \\ x_3 \cdot V_{in}\sin\left(\omega t + \beta_3\right) \end{bmatrix} \tag{4.2}$$

where,

$$\begin{aligned} x_1 &= \sqrt{1 + k_1^2 - 2k_1\sin\left(\theta_1 - \frac{\pi}{6}\right)} \\ x_2 &= \sqrt{k_1^2 + k_2^2 - 2k_1k_2\sin\left(\theta_1 - \theta_2 - \frac{\pi}{6}\right)} \\ x_3 &= \sqrt{1 + k_2^2 - 2k_2\sin\left(\theta_2 - \frac{5\pi}{6}\right)} \end{aligned} \tag{4.3}$$

$$\beta_1 = \tan^{-1}\left(\frac{k_1\cos\left(\theta_1 + \frac{5\pi}{6}\right)}{1 - k_1\sin\left(\theta_1 - \frac{\pi}{6}\right)}\right)$$

$$\beta_2 = \tan^{-1}\left(\frac{k_1\cos\left(\theta_1 + \frac{5\pi}{6}\right) - k_2\cos\left(\theta_2 + \frac{\pi}{6}\right)}{k_1\sin\left(\theta_1 - \frac{\pi}{6}\right) - k_2\sin\left(\theta_2 - \frac{5\pi}{6}\right)}\right) \tag{4.4}$$

$$\beta_3 = \tan^{-1}\left(\frac{k_2 \cos\left(\theta_2 + \frac{\pi}{6}\right)}{k_2 \sin\left(\theta_2 - \frac{5\pi}{6}\right) - 1}\right)$$

For developing the modified DSVM strategy, the direct AC-AC three-phase converter illustrated in Fig 4.1 is considered. Mapping the three-phase sets of electric parameters of the converter to the complex space, the corresponding Park's vectors can be defined:

Input phase voltage

$$\overline{U}_{inp}(t) = (v_a(t) + v_b(t)\cdot e^{j\frac{2\pi}{3}} + v_c(t)\cdot e^{j\frac{4\pi}{3}}) = \left|\overline{U}_{inp}\right|\cdot e^{j\angle\overline{U}_{inp}} \tag{4.5}$$

$$U_{inp0}(t) = (v_a(t) + v_b(t) + v_c(t)) \tag{4.6}$$

Input/output line-to-line voltages

$$\overline{U}_{inl}(t) = (v_{ab}(t) + v_{bc}(t)\cdot e^{j\frac{2\pi}{3}} + v_{ca}(t)\cdot e^{j\frac{4\pi}{3}}) = \left|\overline{U}_{inl}\right|\cdot e^{j\angle\overline{U}_{inl}} \tag{4.7}$$

$$\overline{U}_{outl}(t) = (v_{AB}(t) + v_{BC}(t)\cdot e^{j\frac{2\pi}{3}} + v_{CA}(t)\cdot e^{j\frac{4\pi}{3}}) = \left|\overline{U}_{outl}\right|\cdot e^{j\angle\overline{U}_{outl}} \tag{4.8}$$

Input/output line currents

$$\overline{I}_{in}(t) = (i_a(t) + i_b(t)\cdot e^{j\frac{2\pi}{3}} + i_c(t)\cdot e^{j\frac{4\pi}{3}}) = \left|\overline{I}_{in}\right|\cdot e^{j\angle\overline{I}_{in}} \tag{4.9}$$

$$\overline{I}_{out}(t) = (i_A(t) + i_B(t)\cdot e^{j\frac{2\pi}{3}} + i_C(t)\cdot e^{j\frac{4\pi}{3}}) = \left|\overline{I}_{out}\right|\cdot e^{j\angle\overline{I}_{out}} \tag{4.10}$$

In addition, it is worth noting that for line-to-line voltages the homopolar component is equal to zero. Then, for the input line-to-line vector,

$$\begin{aligned} \mathbf{Re}\left\{\overline{U}_{inl}(t)\right\} &= \frac{3}{2}v_{ab}(t) \\ \mathbf{Im}\left\{\overline{U}_{inl}(t)\right\} &= \sqrt{3}v_{bc}(t) + \frac{\sqrt{3}}{2}v_{ab}(t) \end{aligned} \tag{4.11}$$

Finally the modulus and phase of Park's input line-to-line voltage vector are,

$$\left|\overline{U}_{inl}\right| = \sqrt{3\left(v_{ab}^2(t) + v_{bc}^2(t) + v_{ab}(t)\cdot v_{bc}(t)\right)} \tag{4.12}$$

$$\angle\overline{U}_{inl} = \tan^{-1}\left(\frac{2v_{bc}(t)+v_{ab}(t)}{\sqrt{3}v_{ab}(t)}\right) \tag{4.13}$$

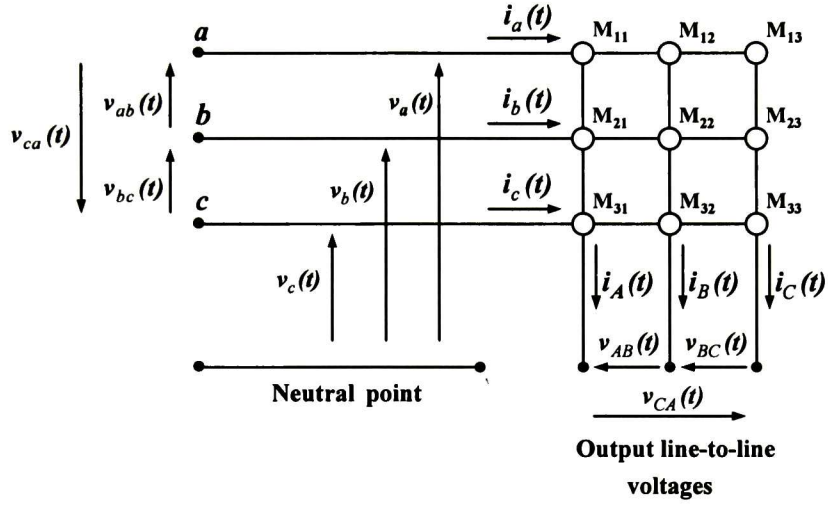


Figure 4.1. Conversion matrix basic structure

By substituting eq. (4.1) within the last expressions all actual unbalanced conditions can be taken into account, where the balanced condition is a particular case.

With the purpose of setting up quantitative indexes among arguments and modulus on Park's vectors ($\overline{U}_{inp}$ and $\overline{U}_{inl}$), expressions defined as a function of the same variables for both vectors are required. Thus, the following relationships arise:

$$\left|\overline{U}_{inp}\right| = \sqrt{v_{ab}^2(t) + v_{bc}^2(t) + v_{ab}(t)\cdot v_{bc}(t)} \tag{4.14}$$

$$\angle\overline{U}_{inp} = \tan^{-1}\left(\frac{\sqrt{3}v_{bc}(t)}{2v_{ab}(t)+v_{bc}(t)}\right) \tag{4.15}$$

Finally,

$$\left|\overline{U}_{inl}\right| = \sqrt{3} \cdot \left|\overline{U}_{inp}\right| \tag{4.16}$$

$$\angle\overline{U}_{inl} = \angle\overline{U}_{inp} + \frac{\pi}{6} \tag{4.17}$$

These two expressions can be satisfied independently of the unbalance degree.

4.2.2 Switching states analysis in Park's complex space for unbalanced conditions

As it is known, in the DSVM control strategy just the fixed and zero vectors are utilized [4.16]. The corresponding Park's vectors $\overline{U}_{out}$ and $\overline{I}_{in}$ under unbalanced conditions are presented in Appendix A. For comparison purposes, analysis for state S2, Fig. 4.2, is developed here.

The input/output voltages relationships become:

$$\begin{aligned} v_{AB}(t) &= 0 \\ v_{BC}(t) &= v_{AB}(t) \\ v_{CA}(t) &= -v_{AB}(t) \end{aligned} \tag{4.18}$$

Then output-voltage Park's vector is,

$$\left|\overline{U}_{outl}(t)\right| = \sqrt{3} \cdot v_{ab}(t) \qquad \angle\overline{U}_{outl}(t) = \frac{\pi}{2} \tag{4.19}$$

For generating a set of balanced output line-to-line voltages in the matrix converter, the input/output relationships of currents are,

$$\begin{aligned} i_a(t) &= i_A(t) + i_B(t) = -i_C(t) \\ i_b(t) &= i_C(t) \\ i_c(t) &= 0 \end{aligned} \tag{4.20}$$

The corresponding Park's vector is,

$$\left|\bar{I}_{in}(t)\right| = \sqrt{3}\cdot i_C(t) \qquad \angle\bar{I}_{in}(t) = \frac{5\pi}{6} \tag{4.21}$$

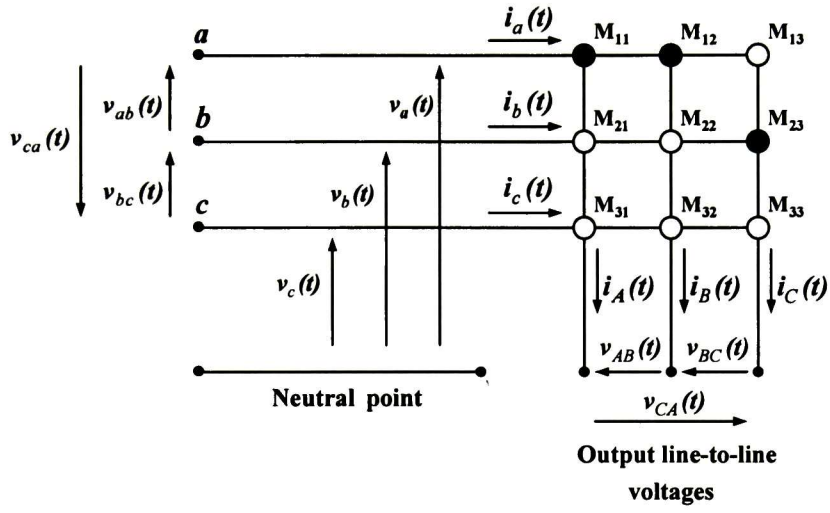


Figure 4.2. Matrix topology for state S2.

The previous analysis shows that the expressions obtained for vectors $\bar{U}_{outl}$ and $\bar{I}_{in}$ under balanced conditions, Table A.1, can be also utilized for the case of unbalanced input conditions just taking into account the voltages defined by eqs. (4.1) and (4.2). The modifications aroused by unbalanced conditions are manifested on the vectors behavior and the magnitude of the output voltages. For instance, fixed vectors during input balanced conditions divide complex space in six sectors forming up a regular hexagon, and the output voltage vector that can be generated for maximum balanced output voltage conditions corresponds to 0.866 times the maximum circle that can be inscribed inside the hexagon, Fig. 4.3a. On the other hand, if sag of 50% is considered on input phase b, fixed vectors still divide the complex space in six sectors; however, now the maximum magnitude of the balanced output voltage that can be generated is reduced by a factor of $^2/_3$ .Such variations have to be considered at the moment of synthesizing the reference Park's vectors.

Taking the output voltage and input current vectors as references, these vectors $\bar{U}_{outl(ref)}$ and $\bar{I}_{in(ref)}$ can be located within any sector, Figs. 4.4 and 4.5.

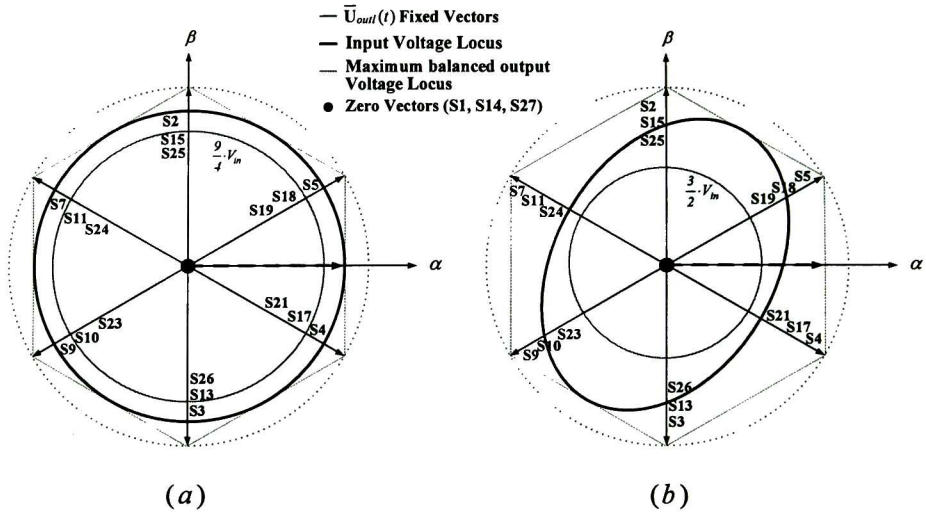


Figure 4.3. (a) Voltage vectors for balanced input voltage condition. (b) Voltage vectors for unbalanced conditions (sag of 50% on phase *b*).

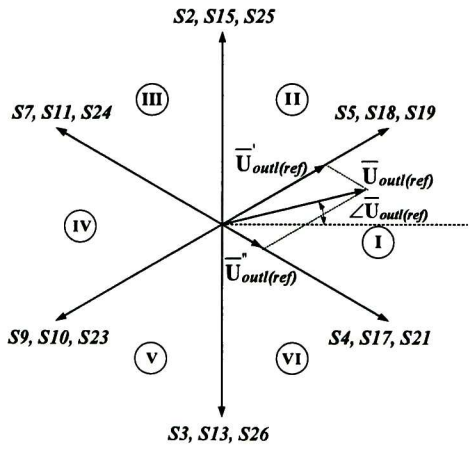


Figure 4.4. Output-voltage's fixed vectors

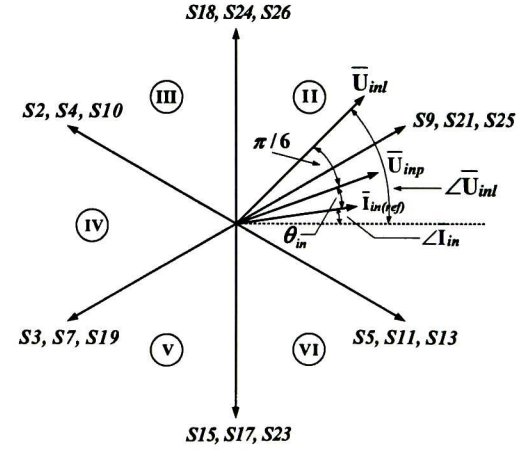


Figure 4.5. Input-current's fixed vectors

The major aim of the strategy is to control the Park's vector of the output voltage $\overline{U}_{outl}$, and to control the phase θ_{in} between the input voltage $\overline{U}_{inp}$ and the input current $\overline{I}_{in}$. This allows:

- Controllable output-voltages, despite input-voltages condition.
- Output voltages and input currents with acceptable harmonic content

- Control of amplitudes and frequency on the output voltages
- Control of input power factor.

4.2.3 Voltage reference tracking

In the following, it is assumed that vectors $\overline{U}_{out(ref)}$ and $\overline{I}_{in(ref)}$ are located within sector I, respectively. In order to determine the line-to-line output voltage, Fig 4.6, the following relationships are used:

$$\overline{U}'_{outl(ref)} = \left(\overline{U}^{I}_{outl} \cdot m_I\right) + \left(\overline{U}^{II}_{outl} \cdot m_{II}\right) \tag{4.22}$$

$$\overline{U}''_{outl(ref)} = \left(\overline{U}^{III}_{outl} \cdot m_{III}\right) + \left(\overline{U}^{IV}_{outl} \cdot m_{IV}\right) \tag{4.23}$$

where m_i represents the commutation-vectors' duty cycle. i.e.,

$$m_i = \frac{T_i}{T_s} \qquad i = \{I, II, III, IV\} \tag{4.24}$$

T_s is the sample time and T_i is the time elapsed while the *i-th* state is *on*.

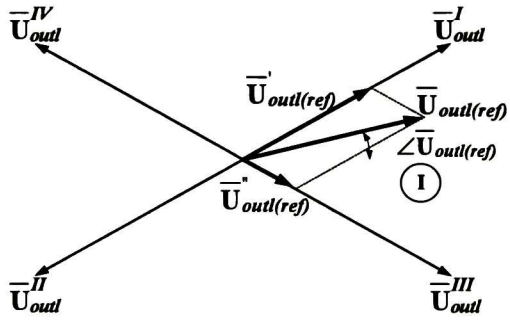


Figure 4.6 $\overline{U}_{out(ref)}$ tracking

After conduct the corresponding vectorial projection on Fig 4.6, the following expressions can be deduced:

$$\overline{U}'_{outl(ref)} = \frac{2}{\sqrt{3}}\left|\overline{U}_{outl(ref)}\right| \cdot \cos\left(\angle\overline{U}_{outl(ref)} - \frac{\pi}{3}\right) \cdot e^{j\frac{\pi}{6}} \tag{4.25}$$

$$\overline{U}''_{outl(ref)} = \frac{2}{\sqrt{3}}\left|\overline{U}_{outl(ref)}\right| \cdot \cos\left(\angle\overline{U}_{outl(ref)} + \frac{\pi}{3}\right) \cdot e^{-j\frac{\pi}{6}} \tag{4.26}$$

From (4.22)-(4.23), (4.25)-(4.26), it is established that:

$$\overline{U}'_{outl(ref)} = \left(\overline{U}^{I}_{outl} \cdot m_I\right) + \left(\overline{U}^{II}_{outl} \cdot m_{II}\right) = \frac{2}{\sqrt{3}}\left|\overline{U}_{outl(ref)}\right| \cdot \cos\left(\angle\overline{U}_{outl(ref)} - \frac{\pi}{3}\right) \cdot e^{j\frac{\pi}{6}} \tag{4.27}$$

$$\overline{U}''_{outl(ref)} = \left(\overline{U}^{III}_{outl} \cdot m_{III}\right) + \left(\overline{U}^{IV}_{outl} \cdot m_{IV}\right) = \frac{2}{\sqrt{3}}\left|\overline{U}_{outl(ref)}\right| \cdot \cos\left(\angle\overline{U}_{outl(ref)} + \frac{\pi}{3}\right) \cdot e^{-j\frac{\pi}{6}} \tag{4.28}$$

From Figs 4.4 and 4.5, it is worth noting that the fixed states have three alternatives (for example, S19, S18, S5) whose modulus varies instantly depending on the line-to-line input voltages. One way to attain the vector $\overline{U}_{outl(ref)}$ is selecting the commutation states with the greatest modulus. As a consequence, the selected commutation states depend on the position of vector $\overline{U}_{inp}$. The argument of $\overline{U}_{inp}$ depends on the line-to-line input voltages as indicated in eq. (4.15). Figure 4.7, illustrates the relationship between the line-to-line input voltages and the sector where the vector $\overline{U}_{inp}$ is located, despite unbalanced degree. Thus, vector $\overline{U}'_{outl(ref)}$ must be constituted by commutation states S5 and S9, while vector $\overline{U}''_{outl(ref)}$ by states S4 and S7, Fig. (4.8).

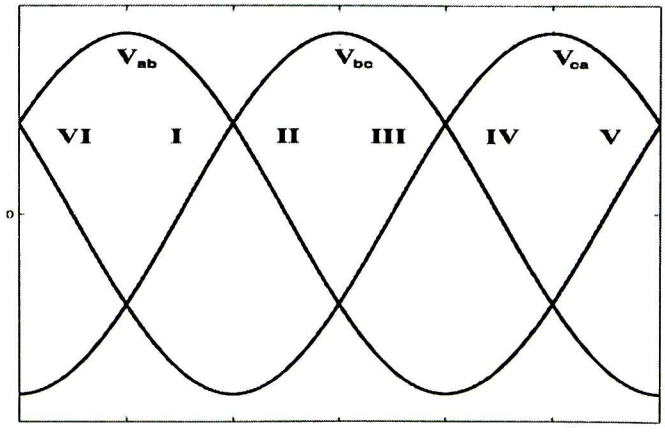


Figure 4.7 Relationship between line-to-line input voltages and $\overline{U}_{inp}$ vector's sectors

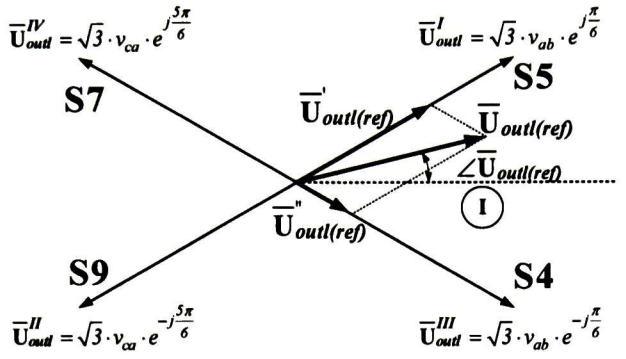


Figure 4.8 Required states for tracking $\overline{U}_{outl(ref)}$ when $\overline{U}_{inp}$ is in sector I.

By defining instantaneous line-to-line input voltages in terms of its Park vector, as:

$$v_{ab}(t) = \frac{2}{3}\left|\overline{U}_{inl}\right|\cos\left(\angle\overline{U}_{inl}\right) \tag{4.29}$$

$$v_{bc}(t) = \frac{2}{3}\left|\overline{U}_{inl}\right|\cos\left(\angle\overline{U}_{inl} - \frac{2\pi}{3}\right) \tag{4.30}$$

$$v_{ca}(t) = \frac{2}{3}\left|\overline{U}_{inl}\right|\cos\left(\angle\overline{U}_{inl} - \frac{4\pi}{3}\right) \tag{4.31}$$

It is possible, from Fig 4.8 and (4.29)-(4.31), to rearrange (4.27) and (4.28) in terms of the line-to-line input voltage vector,

$$\left|\overline{U}_{outl(ref)}\right| \cdot \cos\left(\angle\overline{U}_{outl(ref)} - \frac{\pi}{3}\right) = \left|\overline{U}_{inl}\right|\cos\left(\angle\overline{U}_{inl}\right)m_I - \left|\overline{U}_{inl}\right|\cos\left(\angle\overline{U}_{inl} - \frac{4\pi}{3}\right)m_{II} \tag{4.32}$$

$$\left|\overline{U}_{outl(ref)}\right| \cdot \cos\left(\angle\overline{U}_{outl(ref)} + \frac{\pi}{3}\right) = \left|\overline{U}_{inl}\right|\cos\left(\angle\overline{U}_{inl}\right)m_{III} - \left|\overline{U}_{inl}\right|\cos\left(\angle\overline{U}_{inl} - \frac{4\pi}{3}\right)m_{IV} \tag{4.33}$$

4.2.4 Current reference tracking

Similarly to the previous section, the input reference current $\overline{I}_{in(ref)}$ can be determined, Fig 4.9. It can be established that,

$$\overline{I}'_{in(ref)} = \left(\overline{I}^{II}_{in} \cdot m_{II}\right) + \left(\overline{I}^{IV}_{in} \cdot m_{IV}\right) \tag{4.34}$$

$$\bar{I}''_{in(ref)} = \left(\bar{I}^{I}_{in} \cdot m_I\right) + \left(\bar{I}^{III}_{in} \cdot m_{III}\right) \tag{4.35}$$

Additionally,

$$\bar{I}'_{in(ref)} = \frac{2}{\sqrt{3}}\left|\bar{I}_{in(ref)}\right| \cdot \sin\left(\frac{\pi}{6} + \angle\bar{I}_{in(ref)}\right) \cdot e^{j\frac{\pi}{6}} \tag{4.36}$$

$$\bar{I}''_{in(ref)} = \frac{2}{\sqrt{3}}\left|\bar{I}_{in(ref)}\right| \cdot \sin\left(\frac{\pi}{6} - \angle\bar{I}_{in(ref)}\right) \cdot e^{-j\frac{\pi}{6}} \tag{4.37}$$

From (4.34)-(4.37), and after mathematical manipulations,

$$\frac{2}{\sqrt{3}}\left|\bar{I}_{in(ref)}\right| \cdot \sin\left(\frac{\pi}{6} + \angle\bar{I}_{in(ref)}\right) = \left(\sqrt{3} \cdot i_A \cdot m_{II}\right) - \left(\sqrt{3} \cdot i_B \cdot m_{IV}\right) \tag{4.38}$$

$$\frac{2}{\sqrt{3}}\left|\bar{I}_{in(ref)}\right| \cdot \sin\left(\frac{\pi}{6} - \angle\bar{I}_{in(ref)}\right) = \left(\sqrt{3} \cdot i_A \cdot m_I\right) - \left(\sqrt{3} \cdot i_B \cdot m_{III}\right) \tag{4.39}$$

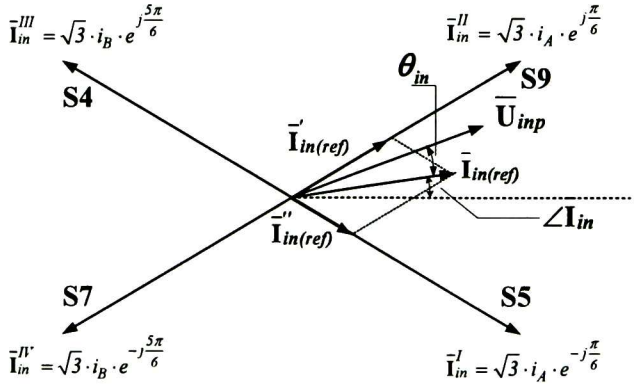


Figure 4.9 $\bar{I}_{in(ref)}$ tracking

In order to avoid the use of current parameters, eqs (4.38)-(4.39) are rewritten as:

$$m_{II} \cdot \sin\left(\frac{\pi}{6} - \angle\bar{I}_{in(ref)}\right) - m_I \cdot \sin\left(\frac{\pi}{6} + \angle\bar{I}_{in(ref)}\right) = 0 \tag{4.40}$$

$$m_{IV} \cdot \sin\left(\frac{\pi}{6} - \angle\bar{I}_{in(ref)}\right) - m_{III} \cdot \sin\left(\frac{\pi}{6} + \angle\bar{I}_{in(ref)}\right) = 0 \tag{4.41}$$

4.2.5 Duty cycles computation

Solving the equation set (4.32)-(4.33) and (4.40)-(4.41) the duty cycles become:

$$m_I = \frac{2}{\sqrt{3}} \cdot \frac{\left|\bar{U}_{outl(ref)}\right|}{\left|\bar{U}_{inl}\right|} \cdot \frac{\cos\left(\angle\bar{U}_{outl(ref)} - \frac{\pi}{3}\right) \cdot \cos\left(\frac{\pi}{3} + \angle\bar{I}_{in(ref)}\right)}{\cos\theta_{in}} \tag{4.42}$$

$$m_{II} = \frac{2}{\sqrt{3}} \cdot \frac{\left|\bar{U}_{outl(ref)}\right|}{\left|\bar{U}_{inl}\right|} \cdot \frac{\cos\left(\angle\bar{U}_{outl(ref)} - \frac{\pi}{3}\right) \cdot \cos\left(\frac{\pi}{3} - \angle\bar{I}_{in(ref)}\right)}{\cos\theta_{in}} \tag{4.43}$$

$$m_{III} = \frac{2}{\sqrt{3}} \cdot \frac{\left|\bar{U}_{outl(ref)}\right|}{\left|\bar{U}_{inl}\right|} \cdot \frac{\cos\left(\angle\bar{U}_{outl(ref)} + \frac{\pi}{3}\right) \cdot \cos\left(\frac{\pi}{3} + \angle\bar{I}_{in(ref)}\right)}{\cos\theta_{in}} \tag{4.44}$$

$$m_{IV} = \frac{2}{\sqrt{3}} \cdot \frac{\left|\bar{U}_{outl(ref)}\right|}{\left|\bar{U}_{inl}\right|} \cdot \frac{\cos\left(\angle\bar{U}_{outl(ref)} + \frac{\pi}{3}\right) \cdot \cos\left(\frac{\pi}{3} - \angle\bar{I}_{in(ref)}\right)}{\cos\theta_{in}} \tag{4.45}$$

The last expressions are valid within the intervals:

$$-\frac{\pi}{6} < \angle\bar{U}_{outl(ref)} < \frac{\pi}{6} \qquad -\frac{\pi}{6} < \angle\bar{I}_{in(ref)} < \frac{\pi}{6} \tag{4.46}$$

Being necessary to verified that:

$$m_I + m_{II} + m_{III} + m_{IV} \leq 1 \tag{4.47}$$

If the sum of duty cycles is less than one, the use of zero states is required.

Substituting (4.42)-(4.45) into (4.47) results,

$$\left|\bar{U}_{outl(ref)}\right| \leq \frac{\sqrt{3}}{2} \cdot \left|\bar{U}_{inl}\right| \cdot \frac{\cos\theta_{in}}{\cos\left(\angle\bar{U}_{outl(ref)}\right) \cdot \cos\left(\angle\bar{I}_{in(ref)}\right)} \tag{4.62}$$

Considering that $\left[\cos\angle\overline{I}_{in(ref)}\right]_{\max}=1$ and $\left[\cos\angle\overline{U}_{outl(ref)}\right]_{\max}=1$, from (4.14) the input/output voltage relationship $\left(q=\frac{V_{out}}{V_{in}}\right)$ can be established:

$$V_{out}\le\frac{1}{3\sqrt{2}}\cdot V_{in}\cdot\left(\sqrt{\gamma+\lambda+\sqrt{\gamma^2+\lambda^2+\varphi^2-2\gamma\lambda}\cdot\sin\left\{2\omega t+\frac{\lambda-\gamma}{\varphi}\right\}}\right)\cdot\cos\theta_{in} \tag{4.63}$$

where,

$$\gamma=x_1\cos(\beta_1)+x_2\cdot k_1\cdot\cos(\beta_2)\cos\left(\theta_1-\frac{2\pi}{3}\right)+x_3\cdot k_2\cdot\cos(\beta_3)\cos\left(\theta_2+\frac{2\pi}{3}\right)$$

$$\lambda=x_2\cdot k_1\cdot\sin(\beta_2)\sin\left(\theta_1-\frac{2\pi}{3}\right)+x_3\cdot k_2\cdot\sin(\beta_3)\sin\left(\theta_2+\frac{2\pi}{3}\right)$$

$$\varphi=-x_1\sin(\beta_1)+x_2\cdot k_1\cdot\sin\left(\beta_2+\theta_1-\frac{2\pi}{3}\right)+x_3\cdot k_2\cdot\sin\left(\beta_3+\theta_2+\frac{2\pi}{3}\right)$$

x_i and β_i (for $i = 1, 2, 3$) are defined in (4.3)-(4.4), and k_1, k_2, θ_1, and θ_2 are used to specify the degree.

From (4.63) it may be observed that $\left|\overline{U}_{in}\right|$ a time variant quantity which depends on the unbalance degree. Besides, it can be noticed that the maximum voltage relationship is reached when $\cos\theta_{in}=1$. Then,

$$V_{out}\le\frac{1}{3\sqrt{2}}\cdot V_{in}\cdot\left(\sqrt{\gamma+\lambda+\sqrt{\gamma^2+\lambda^2+\varphi^2-2\gamma\lambda}\cdot\sin\left\{2\omega t+\frac{\lambda-\gamma}{\varphi}\right\}}\right)_{\max} \tag{4.64}$$

Eq. (4.64) implies that under unbalanced conditions on input voltages, the output-voltage Park's vector is at the most 0.866 times the minimum value of the input voltages Park's vector.

Employing the line-to-line voltages, the following relations are defined:

$$v_{1ab}(t)-v_{1ca}(t)=\frac{2}{\sqrt{3}}\left|\overline{U}_{in}\right|\cos\left(\angle\overline{U}_{in}-\frac{\pi}{6}\right) \tag{4.65}$$

$$v_{1bc}(t) - v_{1ab}(t) = -\frac{2}{\sqrt{3}}\left|\overline{U}_{in}\right|\cos\left(\angle\overline{U}_{in} + \frac{\pi}{6}\right) \tag{4.66}$$

$$v_{1ca}(t) - v_{1bc}(t) = -\frac{2}{\sqrt{3}}\left|\overline{U}_{in}\right|\cos\left(\angle\overline{U}_{in} - \frac{\pi}{2}\right) \tag{4.67}$$

Using (4.17), and taking into account a unitary input power factor $\left(\angle\overline{U}_{inp} = \angle\overline{I}_{in(ref)}\right)$, the duty cycles become:

$$m_I = -\frac{\left|\overline{U}_{outl(ref)}\right|}{\left|\overline{U}_{inl}\right|^2}\cdot\cos\left(\angle\overline{U}_{outl(ref)} - \frac{\pi}{3}\right)\cdot(v_{bc}(t) - v_{ab}(t)) \tag{4.68}$$

$$m_{II} = -\frac{\left|\overline{U}_{outl(ref)}\right|}{\left|\overline{U}_{inl}\right|^2}\cdot\cos\left(\angle\overline{U}_{outl(ref)} - \frac{\pi}{3}\right)\cdot(v_{ca}(t) - v_{bc}(t)) \tag{4.69}$$

$$m_{III} = -\frac{\left|\overline{U}_{outl(ref)}\right|}{\left|\overline{U}_{inl}\right|^2}\cdot\cos\left(\angle\overline{U}_{outl(ref)} + \frac{\pi}{3}\right)\cdot(v_{bc}(t) - v_{ab}(t)) \tag{4.70}$$

$$m_{IV} = -\frac{\left|\overline{U}_{outl(ref)}\right|}{\left|\overline{U}_{inl}\right|^2}\cdot\cos\left(\angle\overline{U}_{outl(ref)} + \frac{\pi}{3}\right)\cdot(v_{ca}(t) - v_{bc}(t)) \tag{4.71}$$

From the above expressions, by incorporating the characteristics of the supply voltage into the computation of the duty cycles makes the modulation process adaptive to the characteristics of the input voltages, hence enabling the output voltages to track closely their reference counterpart even when the supply voltages are non-sinusoidal. The significance of this is that the switching functions of the converter are now varying with variations of the input voltage, while still aiming to track the reference output voltage. This effectively prevents the undesirable features of the supply voltages from propagating on to the output voltages.

4.2.6 Commutation tables

Table 4.1 shows the switching sequences that can be used to avoid multiple switch commutations, based on the proposed optimized double-sided vector sequence presented in [4.18]. Finally the duty cycles can be expressed as indicated in tables 4.2-4.4, where:

- P_I represents the sector where the vector $\bar{I}_{in(ref)}$ is located; as $\cos\theta_{in}=1$, $\left(\angle\bar{U}_{inp}=\angle\bar{I}_{in(ref)}\right)$.
- α_{out} is the angle related to the voltage reference vector, measured from the initial vector of the corresponding sector, Fig. 4.10.

Table 4.1 DSVM vector sequences

CURRENT SECTORS	VOLTAGE SECTORS														
	I					II					III				
	m_I	m_{II}	m_{III}	m_{IV}	m_V	m_I	m_{II}	m_{III}	m_{IV}	m_V	m_I	m_{II}	m_{III}	m_{IV}	m_V
I	S4	S5	S9	S7	S1	S2	S5	S9	S3	E1	S2	S11	S21	S3	S1
II	S9	S7	S17	S18	S27	S9	S3	S15	S18	S27	S21	S3	S15	S24	S27
III	S17	S18	S10	S11	S14	S15	S18	S10	S13	S14	S15	S24	S4	S13	S14
IV	S10	S11	S21	S19	S1	S10	S13	S25	S19	S1	S4	S13	S25	S7	S1
V	S21	S19	S23	S24	S27	S25	S19	S23	S26	S27	S25	S7	S17	S26	S27
VI	S23	S24	S4	S5	S14	S23	S26	S2	S5	S14	S17	S26	S2	S11	S14
	IV					V					VI				
	m_I	m_{II}	m_{III}	m_{IV}	m_V	m_I	m_{II}	m_{III}	m_{IV}	m_V	m_I	m_{II}	m_{III}	m_{IV}	m_V
I	S10	S11	S21	S19	S1	S10	S13	S25	S19	S1	S4	S13	S25	S7	S1
II	S21	S19	S23	S24	S27	S25	S19	S23	S26	S27	S25	S7	S17	S26	S27
III	S23	S24	S4	S5	S14	S23	S26	S2	S5	S14	S17	S26	S2	S11	S14
IV	S4	S5	S9	S7	S1	S2	S5	S9	S3	S1	S2	S11	S21	S3	S1
V	S9	S7	S17	S18	S27	S9	S3	S15	S18	S27	S21	S3	S15	S24	S27
VI	S17	S18	S10	S11	S14	S15	S18	S10	S13	S14	S15	S24	S4	S13	S14

Table 4.2 Duty cycles for P_I = I y IV

P_I = I y IV	
$m_I=(-I)^{P_I}\cdot\frac{\left\|\bar{U}_{outl(ref)}\right\|}{\left\|\bar{U}_{inl}\right\|^2}\cdot\sin\left(\frac{\pi}{3}-\alpha_{out}\right)\cdot\left(v_{bc}(t)-v_{ab}(t)\right)$	(4.72)
$m_{II}=(-I)^{P_I}\cdot\frac{\left\|\bar{U}_{outl(ref)}\right\|}{\left\|\bar{U}_{inl}\right\|^2}\cdot\sin\left(\alpha_{out}\right)\cdot\left(v_{bc}(t)-v_{ab}(t)\right)$	(4.73)
$m_{III}=(-I)^{P_I}\cdot\frac{\left\|\bar{U}_{outl(ref)}\right\|}{\left\|\bar{U}_{inl}\right\|^2}\cdot\sin\left(\alpha_{out}\right)\cdot\left(v_{ca}(t)-v_{bc}(t)\right)$	(4.74)
$m_{IV}=(-I)^{P_I}\cdot\frac{\left\|\bar{U}_{outl(ref)}\right\|}{\left\|\bar{U}_{inl}\right\|^2}\cdot\sin\left(\frac{\pi}{3}-\alpha_{out}\right)\cdot\left(v_{ca}(t)-v_{bc}(t)\right)$	(4.75)

Table 4.3 Duty cycles for P_I = II y V

P_I = II y V	
$m_I = (-1)^{P_I} \cdot \frac{\lvert \overline{U}_{outl(ref)} \rvert}{\lvert \overline{U}_{inl} \rvert^2} \cdot \sin\left(\frac{\pi}{3} - \alpha_{out}\right) \cdot \left(v_{ab}(t) - v_{ca}(t)\right)$	(4.76)
$m_{II} = (-1)^{P_I} \cdot \frac{\lvert \overline{U}_{outl(ref)} \rvert}{\lvert \overline{U}_{inl} \rvert^2} \cdot \sin\left(\alpha_{out}\right) \cdot \left(v_{ab}(t) - v_{ca}(t)\right)$	(4.77)
$m_{III} = (-1)^{P_I} \cdot \frac{\lvert \overline{U}_{outl(ref)} \rvert}{\lvert \overline{U}_{inl} \rvert^2} \cdot \sin\left(\alpha_{out}\right) \cdot \left(v_{bc}(t) - v_{ab}(t)\right)$	(4.78)
$m_{IV} = (-1)^{P_I} \cdot \frac{\lvert \overline{U}_{outl(ref)} \rvert}{\lvert \overline{U}_{inl} \rvert^2} \cdot \sin\left(\frac{\pi}{3} - \alpha_{out}\right) \cdot \left(v_{bc}(t) - v_{ab}(t)\right)$	(4.79)

Tabla 4.4. Duty cycles for P_I = III y VI

P_I = III y VI	
$m_I = (-1)^{P_I} \cdot \frac{\lvert \overline{U}_{outl(ref)} \rvert}{\lvert \overline{U}_{inl} \rvert^2} \cdot \sin\left(\frac{\pi}{3} - \alpha_{out}\right) \cdot \left(v_{ca}(t) - v_{ab}(t)\right)$	(4.80)
$m_{II} = (-1)^{P_I} \cdot \frac{\lvert \overline{U}_{outl(ref)} \rvert}{\lvert \overline{U}_{inl} \rvert^2} \cdot \sin\left(\alpha_{out}\right) \cdot \left(v_{ca}(t) - v_{ab}(t)\right)$	(4.81)
$m_{III} = (-1)^{P_I} \cdot \frac{\lvert \overline{U}_{outl(ref)} \rvert}{\lvert \overline{U}_{inl} \rvert^2} \cdot \sin\left(\alpha_{out}\right) \cdot \left(v_{ab}(t) - v_{ca}(t)\right)$	(4.82)
$m_{IV} = (-1)^{P_I} \cdot \frac{\lvert \overline{U}_{outl(ref)} \rvert}{\lvert \overline{U}_{inl} \rvert^2} \cdot \sin\left(\frac{\pi}{3} - \alpha_{out}\right) \cdot \left(v_{ab}(t) - v_{ca}(t)\right)$	(4.83)

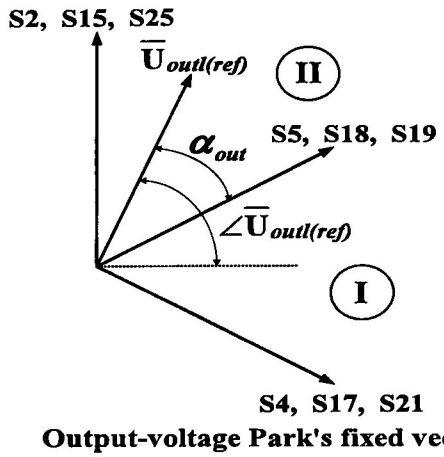


Figure 4.10 α_{out} definition.

4.3 Matrix converter with the modified DSVM simulations

To verify the time domain performance of the matrix converter when is controlled by the MDSVM, numerical simulations are carried out. The converter is analyzed under different operating conditions using PSCAD software. The system key parameters used in the simulations are given in table 4.5. The overall system architecture, as well as the computation process to implement the MDSVM strategy is exposed in Fig. 4.11. It is important to mention that, in order to appreciate the matrix converter characteristic waveforms, no input /output filter was used in this study.

Table 4.5. List of parameters

Parameter	Value
F_s: Switching frequency	6 kHz
V_{in}: Maximum phase input voltage value	$\sqrt{2} \cdot 120$
$f_{in} = f_{out}$: Input / output frequency	60 Hz
L - R: Inductance – Resistance Load	10mH / 10Ω

Departing from the input phase-voltage measurements, the sector K_I (where the vector $\overline{U}_{inp}$ is located) is calculated. As unity power factor is considered, $\overline{U}_{inp} = \overline{I}_{in(ref)}$. Likewise, from the reference voltages, the sector K_V and the angle α_{out} are definite. From table 4.1 the switching pattern is obtained and the duty cycles are computed from the equations expressed in Tables 4.2-4.4, using the values of K_I, α_{out}, and the line-to-line input voltages.

Finally, with the switching states and duty cycles it is possible to establish the state in every switch of the matrix converter, during the actual switching period.

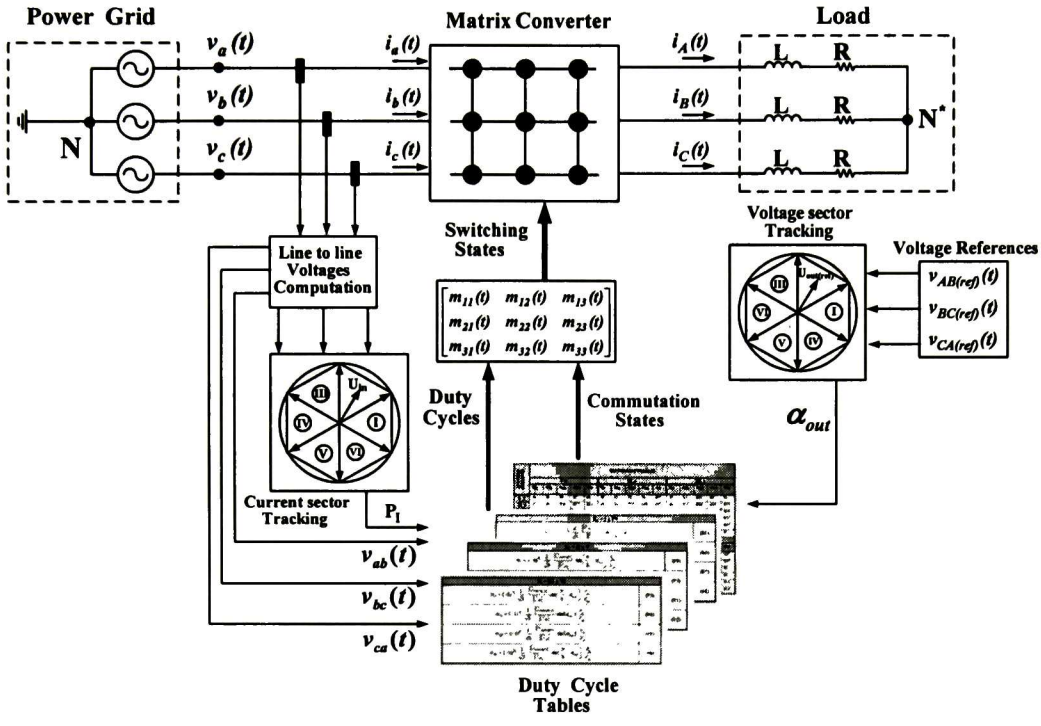


Figure 4.11. System architecture to simulate the modified DSVM control algorithm.

4.3.1 Condition I: Unbalanced Input Voltage

The performance of the MDSVM under unbalanced input voltages is evaluated through a test with the next input conditions: $v_a = V_{in} \angle 0$, $v_b = 1.5 \cdot V_{in} \angle \pi/2$ and $v_c = 0.5 \cdot V_{in} \angle -\pi/3$. The expected output voltages have to be a set of three-phase balanced voltages. Fig. 4.12 shows Park's vectors $\overline{U}_{inl}$ and $\overline{U}_{outl(ref)}$ in the complex space. From this figure, it can be appreciated that the voltage imbalance limits the output voltages according to eq. (4.64). Under this condition $|V_{outp}|_{\max} \approx 0.4 \cdot |V_{inp,nominal}|$

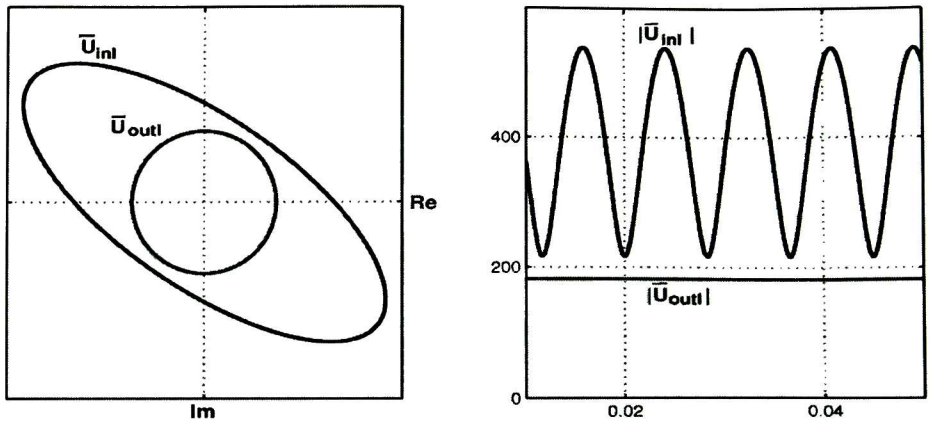


Figure 4.12. From left to right: $\overline{U}_{inl}$ and $\overline{U}_{outl(ref)}$ Park vectors in the complex space, Vectors magnitude.

Input and output phase voltages are depicted in Fig. 4.13. Since no passive filters have been employed, output-voltage harmonic content is relatively high but harmonics are concentrated around the vicinity of the switching frequency and its multiples. Thus, by increasing the switching frequency, harmonics order also will increase making them easier to filter out.

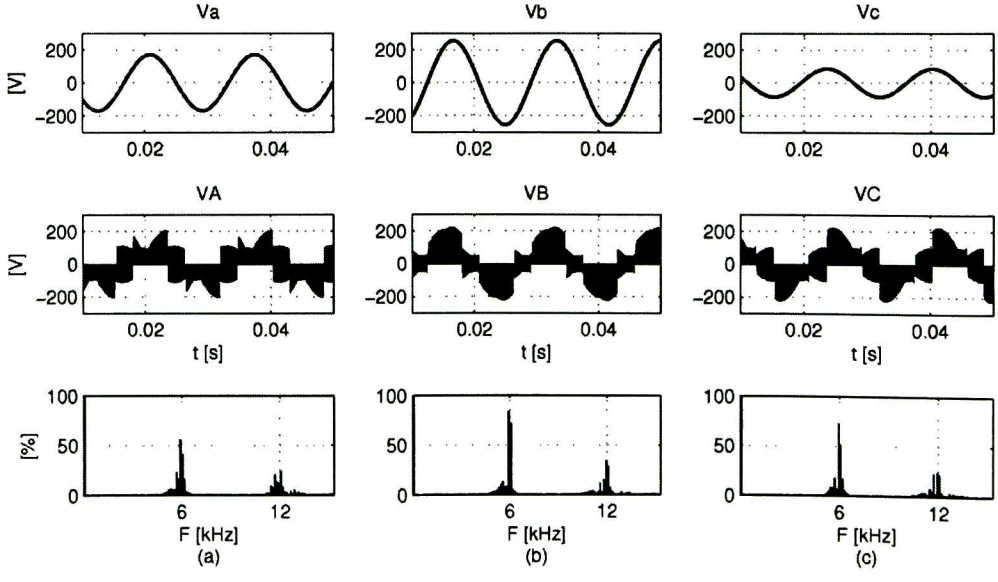


Figure 4.13. From Top to bottom: Input phase voltages, Output phase voltages and output voltage harmonic spectrum (as percent of the fundamental component). a)Phase *a*, b) Phase *b*, c) Phase *c*.

In Fig. 4.14, a similar analysis is presented for the currents. In a similar way as voltages, input currents shows harmonic components of considerable magnitude around the commutation frequency, but the inductive nature of the load has filter the load currents which are practically sinusoidal. Finally, the comparison exhibited in Fig. 4.15 shows that despite the substantial degree of imbalance in the supply voltages, the proposed modulation strategy has no problem in synthesized effectively the voltage reference imposed which can be verified through the load currents.

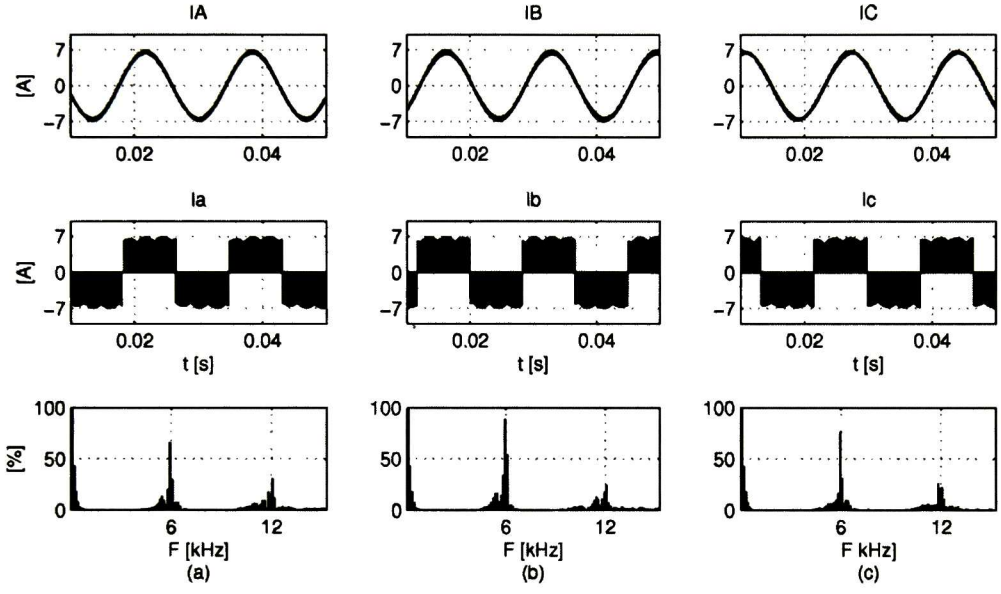


Figure 4.14. From Top to bottom: Output currents, Input currents and Input currents harmonic spectrum (as percent of the fundamental component).). a) Phase *a*, b) Phase *b*, c) Phase *c*.

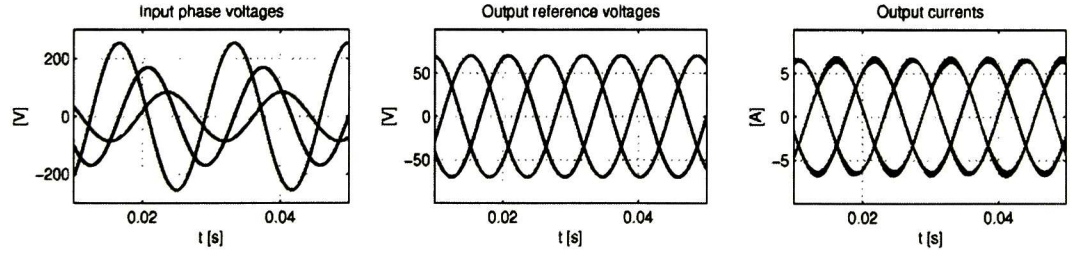


Figure 4.15. From left to right: Input phase voltages, Output voltage references and Output currents

4.3.2 Condition II: Distorted input voltage

The next step in the evaluation of the MDSVM is to analyze the converter behavior against another adverse condition commonly presented in distribution systems, the presence of voltage harmonic components. For this study case, 5^{th} and 7^{th} harmonic components of different magnitudes have been added to the phase voltages as follows: 0.5 and 0.1 on phase *a*, 0.3 and 0.3 on phase *b*, 0.4 and 0.2 on phase *c*, this values are related to the magnitude of the fundamental component of phase *a*.

In this case, for a balance output set of voltages the maximum output voltage magnitude is restricted to 0.7 times the nominal value of the input voltage, as Fig. 4.16 illustrates.

In Fig 4.17, input voltages show the distorted waveform expected by the addition of the harmonic components. The low order components added are no longer presented in the output signals, which only show the harmonic spectrum caused by the modulation scheme. It is worth noting that by reducing the imbalance degree, the magnitudes of harmonic components in the output voltages are even lower than they were in the previous case. Currents shows a similar behavior as in the study case analyzed before; again, the output currents are practically pure sinusoidal. In contrast, input currents shows the matrix converter characteristic waveforms, low order harmonics of magnitude less than 7% still remains after voltage compensation.

By means of the output currents, it is verified that even under considerably distortion in the supply voltages, the control strategy does not exhibit problems to synthesize the reference voltages provided the restrictions imposed by the algorithm are fulfilled, Fig. 4.19.

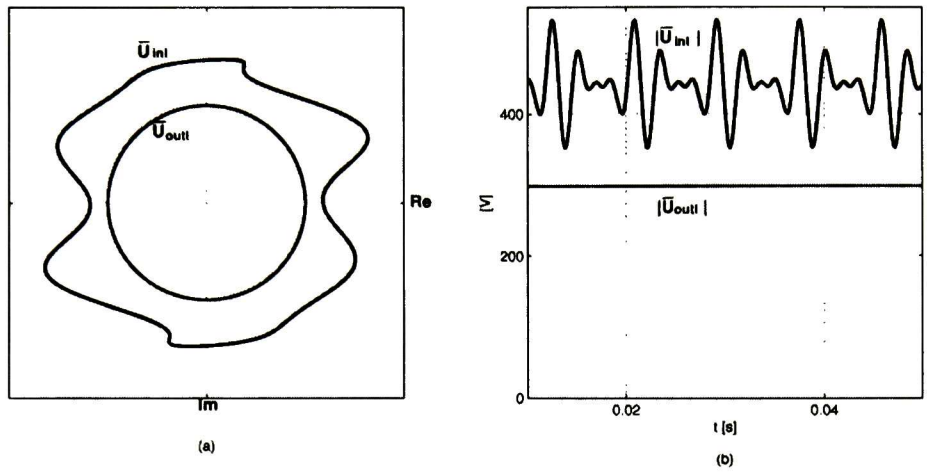


Figure 4.16. a) $\overline{U}_{inl}$ and $\overline{U}_{outl(ref)}$ Park vectors in the complex space. b) Vectors magnitude.

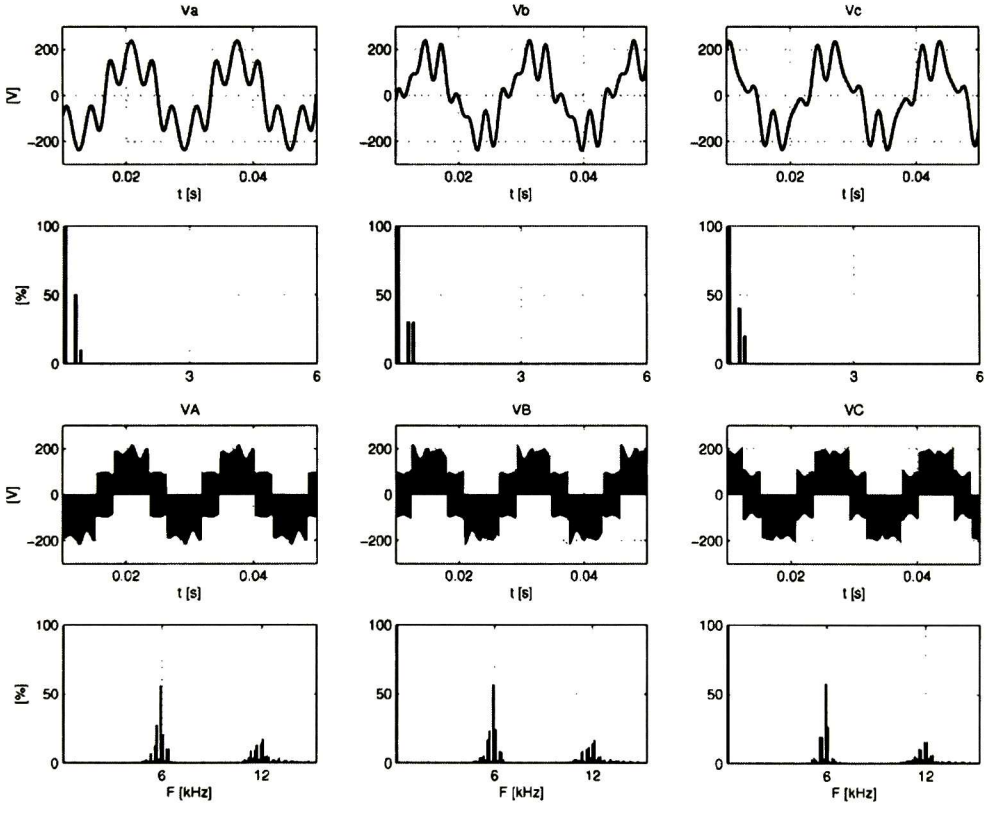


Figure 4.17. From Top to bottom: Input phase voltages, input voltages harmonic spectrum, output phase voltages and output voltage harmonic spectrum. (Harmonics expressed as percent of the fundamental component).

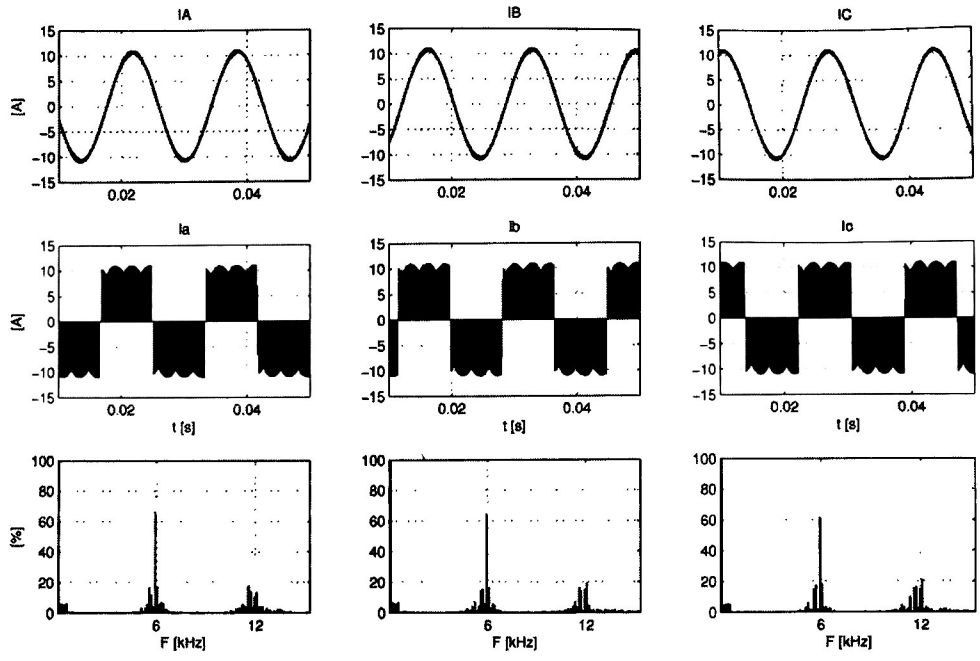


Figure 4.18. From Top to bottom: Output currents, Input currents and Input currents harmonic spectrum (as percent of the fundamental component).

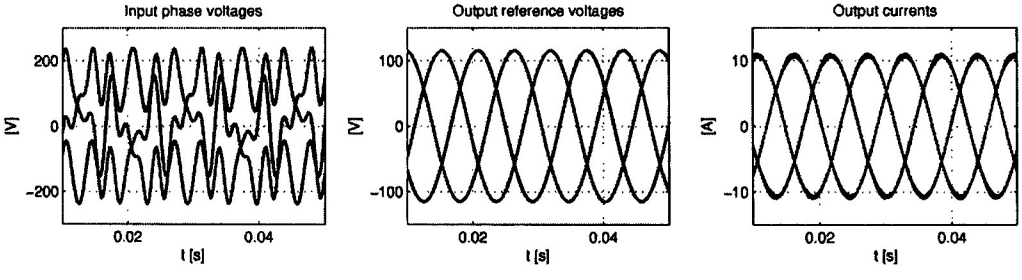


Figure 4.19. From left to right: Input phase voltages, Output voltage references and Output currents

4.4 Experimental results

The hardware validation of the proposed modulation strategy was conducted on a matrix converter laboratory-scale prototype property of the Institute of Energy Technology of Aalborg University. The matrix converter topology is illustrated in Fig. 4.20.

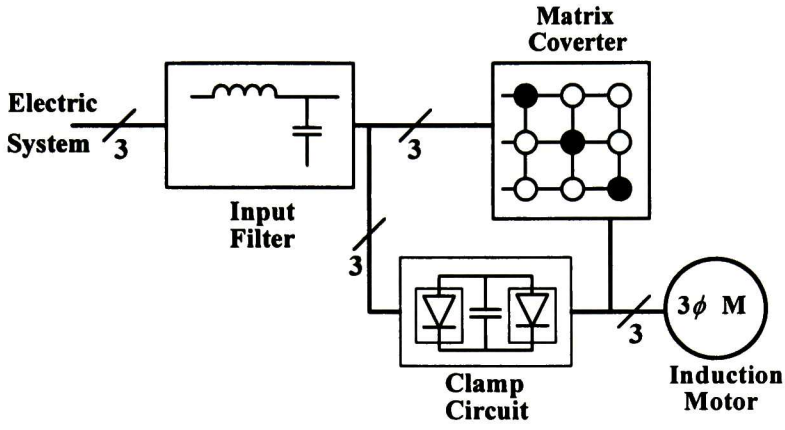


Figure 4.20. Schematic diagram of the matrix converter prototype

The main characteristics of the prototype are listed:

- Matrix converter power stage consists of three power modules 3ϕ-1ϕ with IGBT's of 1200V/25A
- Input filter components: Inductance per phase of 1.2 mH/10 Apk type B82505-W-A4 (S-M) and capacitance per phase of 6X1 μF/250 V (class X2) type PHE 830MF7100M (Evoxrifa).
- The Clamp circuit was built with diodes BYPT 12PI-1000, V_{rrm} = 1000 V, I_{fsm} = 12 A, I_{frm} = 150 A, and a capacitor of 9.4 μF/1050 V_{dc} snubber type.

The proposed MDSVM strategy was implemented in a digital signal processor (DSP) of 32-bit floating point from Analog Devices (ADSP 21062). DSP board is internally connected to a control PC in order to improve the data storage capability. Data acquisitions are made through an AD board of 8 channels, 12 bits. A control board based on SAB 80C167 microcontroller from Siemens is employed to generate all the time signals required for the system. The system control diagram is shown in Fig. 4.21.

For the experimental tests the programmable AC Power Source 15003iX from California Instruments as utilized for disturbance generation. Likewise, the matrix converter is supplied by a 4 kVA autotransformer and is connected as driver of a 4 kW induction motor which is mechanically coupled with a DC machine. An image of the overall system is presented in Fig. 4.22.

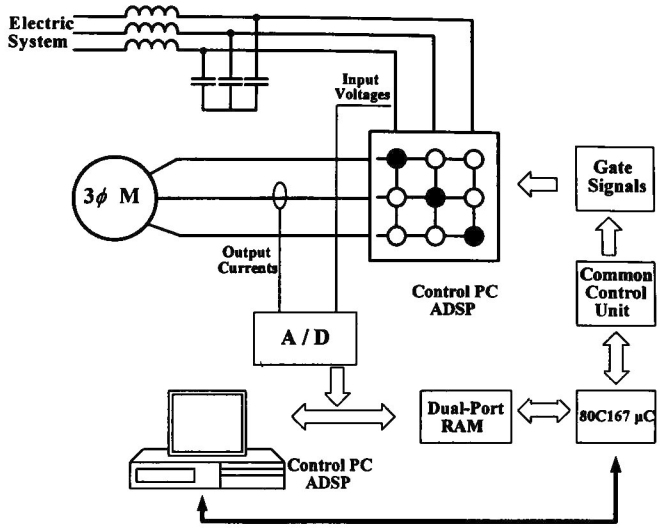


Figure 4.21. Schematic diagram of the matrix converter control system.

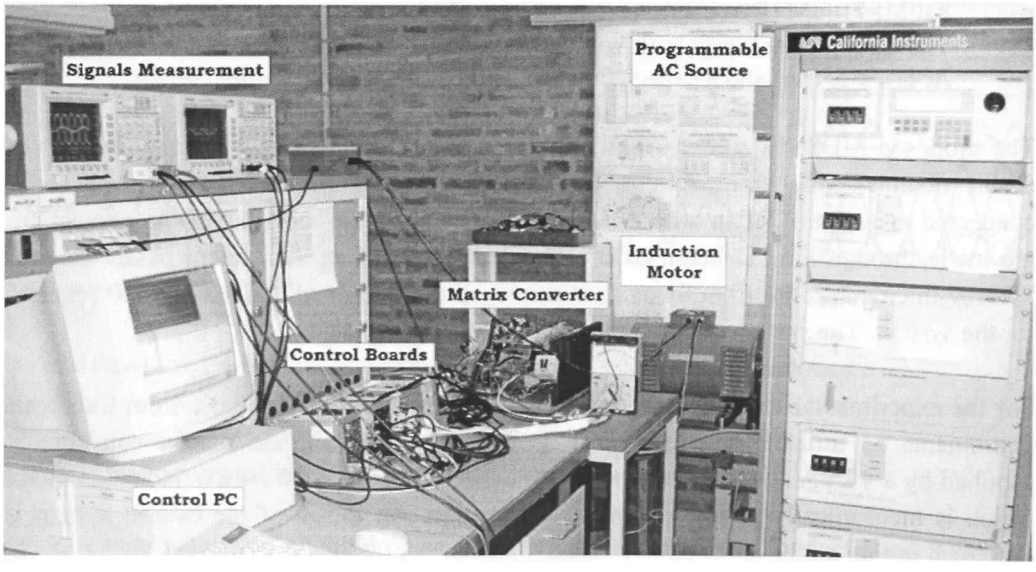


Figure 4.22. Image of the matrix converter prototype. (Laboratory of the Institute of Energy Technology, Aalborg University, Denmark).

With the purpose of validate the modulation strategy proposed, several experimental tests were carried out. The first one was made under nominal input conditions, balanced input voltages at 50 Hz and a switching frequency of 6.5 kHz. Fig. 4.23 shows the main motor

signals under this condition. The harmonic content in the input and output currents on matrix converter is very low as expected. Furthermore, the unity power factor can be verified in the figure.

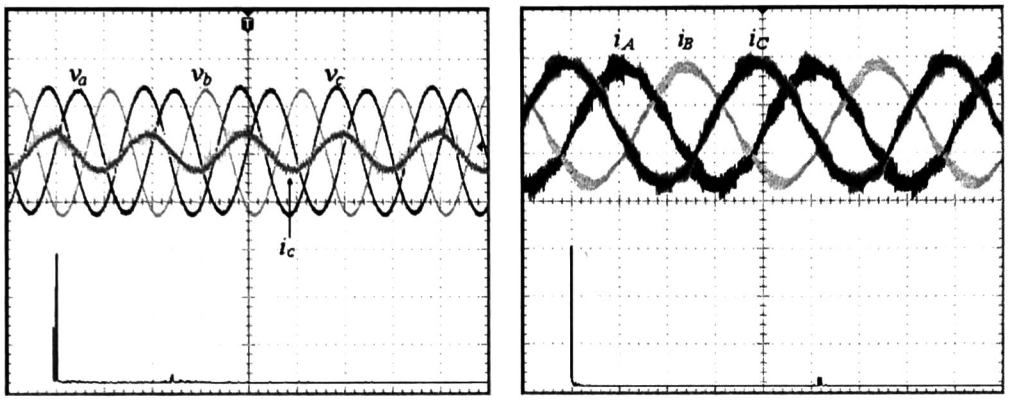


Figure 4.23. a) Input voltages (100V/div, 10ms/div), Phase *c* Input current (2A/div, 10ms/div) and input current FFT (200mA/div, 625 Hz/div). b) Output currents (1A/div, 10ms/div) and phase *a* output current FFT (250mA/div, 1.25 kHz/div).

The characteristic output voltage waveforms can be appreciated in Fig. 4.24, in which it can be seen that the output voltage only contains harmonic components at the switching frequency and its multiples.

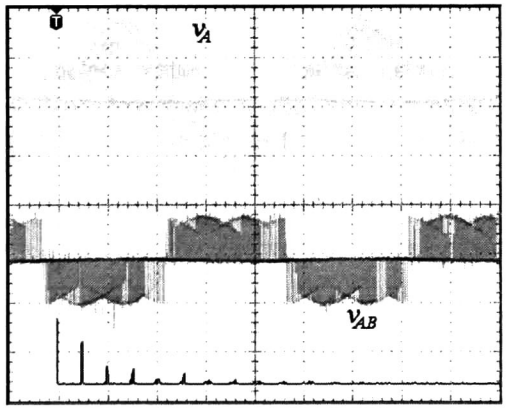
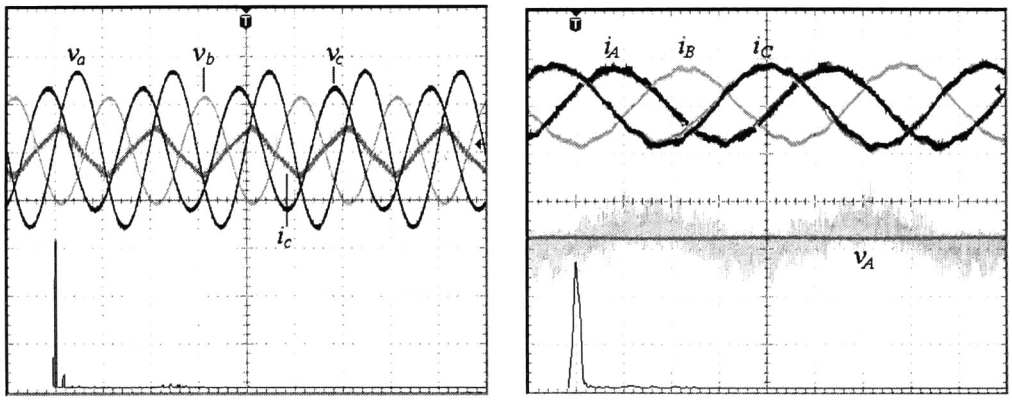


Figure 4.24. Phase *a* output voltage (50V/div, 4ms/div), Line-to-line output voltage (250V/div, 4ms/div). Bottom: Phase voltage FFT (50V/div, 12.5 kHz/div)

In the second test, performance of matrix converter under unbalanced input voltages condition is evaluated. Input voltages of 165 V_{peak}, 127 V_{peak} and 113 V_{peak} were utilized. Results are presented in Fig. 4.25. The supplied voltages contain a 12.83 % of imbalance,

according to the definition found in NEMA standard MG1 [4.18]. Despite the high imbalance degree presented at the input terminals, the output currents just exhibit an unnoticeable percent of imbalance plus a slight distortion produced by the SVM over-modulation, but as the FFT indicates not any considerable harmonic component is present in the output voltage. At this voltage level, the small variations on the output signals complicate the precise calculation of imbalance percent therefore NEMA's criterion cannot be considered. Anyway, the improvement obtained on the system performance is undeniable.



(a) (b)

Figure 4.25. a) Input voltages (100V/div,10ms/div),Phase *c* input current (2A/div, 10ms/div) and input current FFT (200mA/div, 625 Hz/div). b) Output currents (1A/div, 10ms/div), Phase *a* output voltage (50V/div, 10ms/div). Bottom: Phase *a* output current FFT (200mA/div, 125 Hz/div).

In the last case analyzed, the input voltages have the next characteristics:

- V_a: Fundamental component of 100 V with a 5th harmonic component of 5 V with a phase angle of 355 degrees and a 7th harmonic component of 3 V with a phase angle of 173 degrees. THD = 6%.
  V_b: Fundamental component of 90 V with a 5th harmonic component of 45 V with a phase angle of 356 degrees. THD = 45%.
  V_c: Fundamental component of 98 V with a 5th harmonic component of 15 V with a phase angle of 175 degrees. THD = 15%.

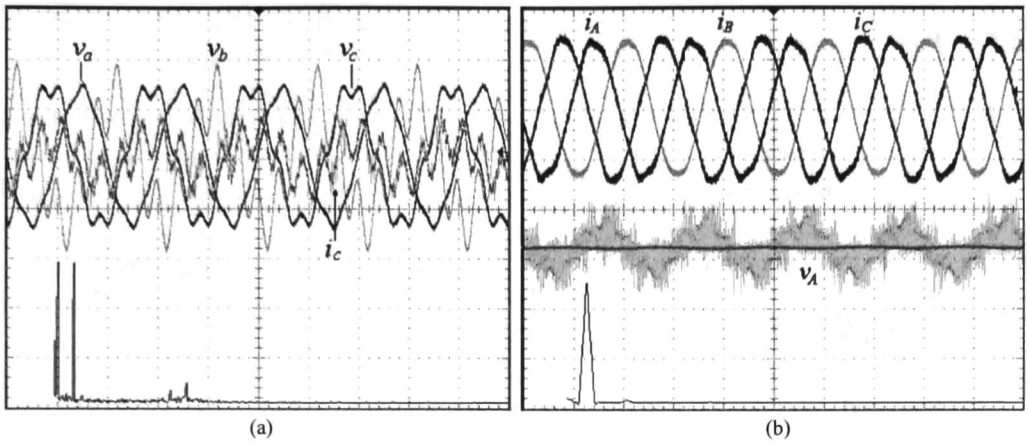


Figure 4.26. a) Input voltages (100V/div,10ms/div), Phase *c* input current (2A/div,10ms/div) and input current FFT (200mA/div,625 Hz/div). b) Output currents (1A/div, 10ms/div), Phase *a* output voltage (50V/div, 10ms/div). Bottom: Phase *a* output current FFT (400mA/div,125 Hz/div).

The results obtained are shown in Fig. 4.26. The current waveforms confirm the effectiveness of the proposed modulation. The output currents have a slight distortion caused by the over modulation introduced.

4.5 Conclusions

In the present chapter the novel MDSVM strategy has been proposed in order to control the matrix converter output voltages. The modulation technique was developed based on the vectorial analysis of the output voltages and input currents in the complex space, considering a set of unbalanced voltages at the input terminals of the converter. The modified duty cycles incorporate the characteristics of the supply voltage into the computations and adjusting the calculated ratios accordingly. This makes the modulation process adaptive to the characteristics of the input voltages.

Simulation and experimental results show that the new method is able to synthesize the desired reference voltages even when the supply voltages are unbalanced and/or distorted. In conclusion, the results presented not only improve the performance of the converter when operates as a driver for induction motors, but now its operational features have been enhanced through the incorporation of the MDSVM, making it suitable for voltage compensation applications.

4.6 References

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CHAPTER V

Matrix Converter-Based Voltage Compensator

Once that power quality issues and their adverse effects on power systems have been addressed, as well as conventional and novel topologies for mitigation devices have been reviewed, in this chapter two DVR topologies will be proposed. From the literature review, it is well known that the DVR has gained industrial acceptation as voltage compensator, mainly motivated by the high economical losses that represent the damage of sensitive equipments. Notwithstanding DVR technology is well established nowadays, the development of novel multi-functional topologies with improved characteristics and lower costs must continue.

In the previous chapter the improved features of the matrix converter under the proposed MDSVM control shows that the compensation voltage application is well suited for this converter, which leads to the topologies proposed in the present chapter.

5.1 DVR Operational Principle

The DVR is one of the CUPS devices that use the power electronics technology, especially inverter technology and is configured as a series connected voltage controller. A schematic diagram of a conventional DVR incorporated into a distribution network is shown in Fig. 5.1. v_s represents the supply system voltage, v_{pcc} is the voltage at the point of common coupling before compensation, v_{load} is the load voltage after compensation, v_{dvr} is the series injected voltage of the DVR, i_s is the current demanded to the supply and i_{load} is the current drawn by the load.

The restorer typically consists of an injection transformer, the secondary winding of which is connected in series with the distribution line, a pulse-width modulated (PWM) voltage

source inverter (VSI) bridge connected to the primary side of the injection transformer and an energy storage device connected at the dc-link of the inverter bridge [5.1]. To control the voltage on the load, the inverter injects the missing voltage in series with the system voltage, using self-commutable electronic switches such as an insulated gate bipolar transistor (IGBT), Fig. 5.2.

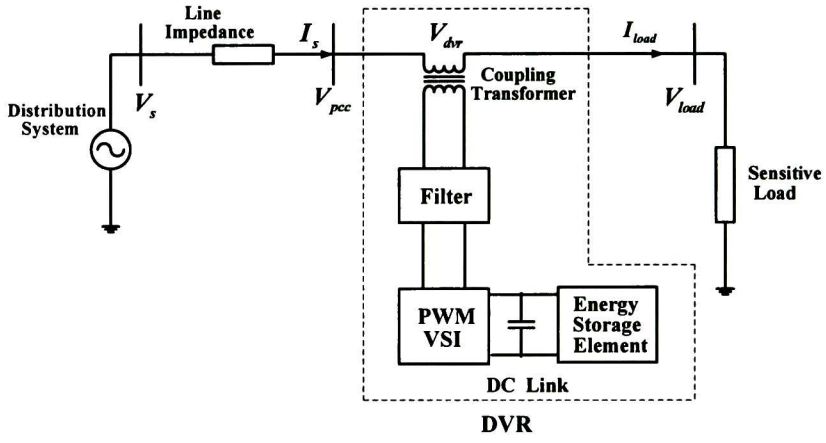

Figure 5.1. Typical schematic of a power distribution system compensated by a DVR

The series injected voltage of the DVR is synthesized by modulating pulse widths of the inverter switches, being necessary to filter the voltage in order to mitigate the switching frequency harmonics generated by the inverter.

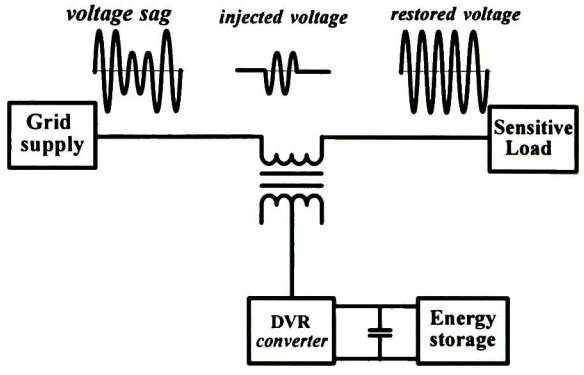

Figure 5.2. Operational principle of a dynamic voltage restorer (DVR)

The injection of an appropriate voltage in the face of an up-stream voltage disturbance requires a certain amount of real and reactive power supply from the DVR. It is quite usual for the real power requirement of the DVR be provided by the energy storage device in the

form of a battery, a capacitor bank or a fly-wheel [5.2]. In some DVR topologies, there is a shunt connected auxiliary providing energy in the DC-link [5.3]. The reactive power requirement is generated by the inverter.

Power requirements on a DVR depend on the scheme utilized for injecting the compensating voltage. For instance, when the injecting voltage has the same phase angle of the distribution system voltage, the magnitude of the injected voltage is small, but a large active power is required. In the case of phase invariant voltage injection scheme, the DVR injects the missing voltage that keeps the magnitude of the voltage as well as the phase of the supply voltage. This scheme needs a large injected voltage and may cause over injection of reactive power. Finally, if the injected voltage is in quadrature with the load current, the DVR does not inject active power. This scheme is highly dependent on the load power factor and can generate a sudden jump of the voltage phase angle. To avoid sudden phase angle jump, the phase of the injected voltage should be gradually changed at the beginning of the compensation as well as at the restoration in order to do not disturb the operation of sensitive loads.

A DVR located between the supply and critical loads, has demonstrated excellent dynamic capability for mitigating voltage sags or swells. Each phase can be controlled independently, and the DVR can adjust the magnitude of the load voltage and the voltage phase angle as well. The advantages of the DVR are its fast response and ability to compensate for a voltage sag and a voltage phase shift using an inverter system. However, DVRs are relatively expensive because of the inverter system, the coupling transformer and mainly by the energy storages that need to contain energy to supply active and reactive power for the missing voltage.

5.2 DVR Topologies

As stated above, conceptually DVRs operate to maintain the load supply voltage at its rated value. During a voltage sag, the DVR injects a voltage to restore the load supply voltages. In this mode the DVR exchanges active and reactive power with the surrounding system. If active power is supplied to the load from the DVR, it needs a source for this energy. Since the first DVR introduced in 1994, several topologies have been developed, along with different control methods and with harmonic compensation purposes [5.4]-[5.5].

Most of the DVR topologies presented in the literature can be classified within two categories:

- DVRs using stored energy devices (batteries, capacitors, flywheel, etc.) to supply the delivered power.

- DVRs having no significant internal energy storage

In the latter case, the energy is taken from the faulted grid supply.

5.2.1 DC Link-based DVR topologies

In [5.6] a detailed comparison of four DVR topologies, Fig. 5.2, is presented. These topologies share one same specific characteristic: the DC-link.

According to the results reported, each DVR topology varies in complexity, performance and cost. From this analysis, the no energy storage DVR topology with a load-side connected passive converter, Fig 5.3b, has been evaluated as the best, followed by the stored energy topology with constant dc-link voltage, Fig. 5.4b. The poorest performance is achieved by the no energy storage topology with a supply side connected passive converter, Fig 5.3a.

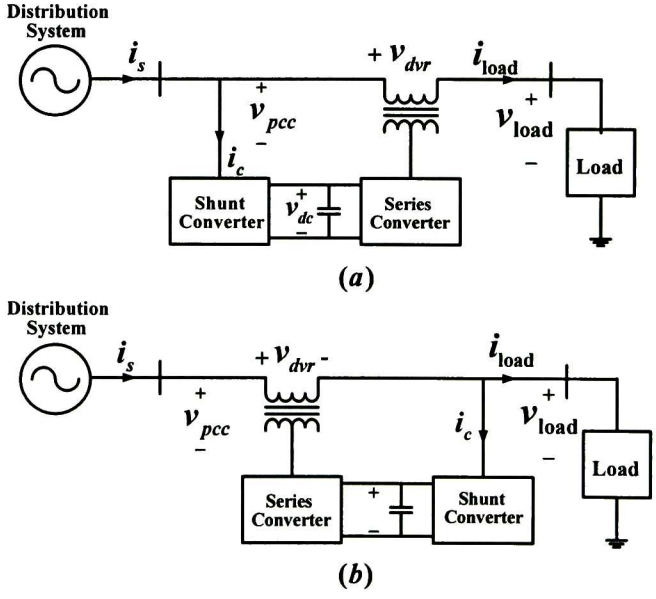

Figure 5.3. DVR topologies with no energy storage. a) Supply side connected converter. b) Load side connected shunt converter

DVR with energy storage and variable DC-link voltage is the simplest topology and consequently the less expensive; however, presents a relatively poor performance for severe and long duration sags. On the other hand, DVR with energy storage and constant dc-link voltage has an excellent performance, particularly for deep voltage sags, but with significant drawbacks regarding complexity, and overall cost. Those reasons disqualify the

two DVR topologies with energy storage, according to the objectives planted at the beginning of this investigation.

Regarding the topologies with no energy storage, the load side connected shunt converter is an excellent alternative with a generally high performance and relatively low cost and complexity. The main drawback of this topology could be the negative grid effects caused by the distorted current drawn by the dc-ac converter. The second topology with no energy storage, the one with the supply side connected converter has the highest number of negative attributes. The particular issues of concern are related to the dc-link performance. The latter topologies' drawbacks could be eliminated by substituting the conventional converter technology.

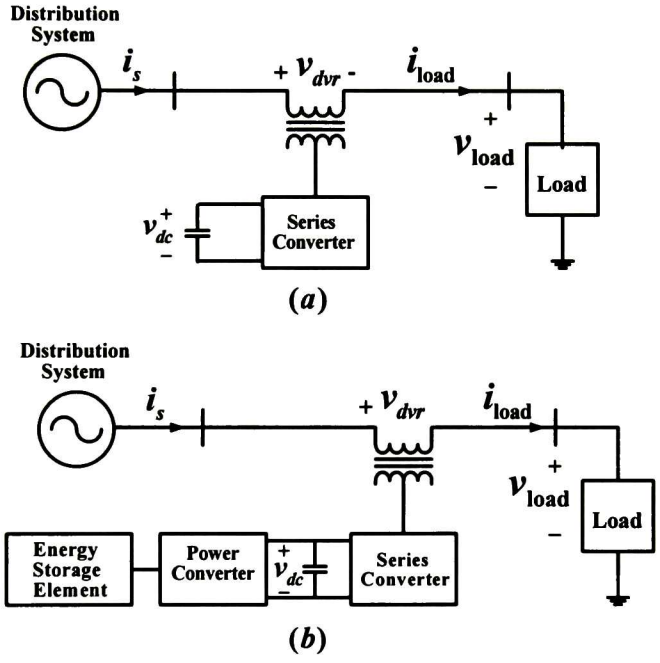

Figure 5.4. DVR topologies with energy storage. a) Variable DC-link voltage. b) With constant DC-link voltage

5.2.2 AC-AC converter-based DVR topologies

In order to eliminate the drawbacks imposed by the use of DC-link passive elements some researchers have focused their efforts on the topologies based on AC-AC power converters, which results in reduced maintenance requirements and improved power density [5.7]-[5.10].

Similarly to the DC-link based topologies, in DVRs with AC-AC converters there are two types of system to be considered. The first one, Fig. 5.5, has not significant energy storage. DVR topologies without external energy devices assume that a part of the supply voltage remains during the sag, and this residual supply can be used to generate the energy required to maintain full load power at rated voltage. Hence, the ability to compensate deep voltage sags will be limited by the input voltage. For instance, in [5.10] a VeSC-based DVR with this topology is proposed to mitigate symmetric voltage sags. Other examples of this technology are found in [5.11] and [5.12], where ac link-based voltage compensators with no energy storage and with a reduced number of power switches are proposed for sags mitigation.

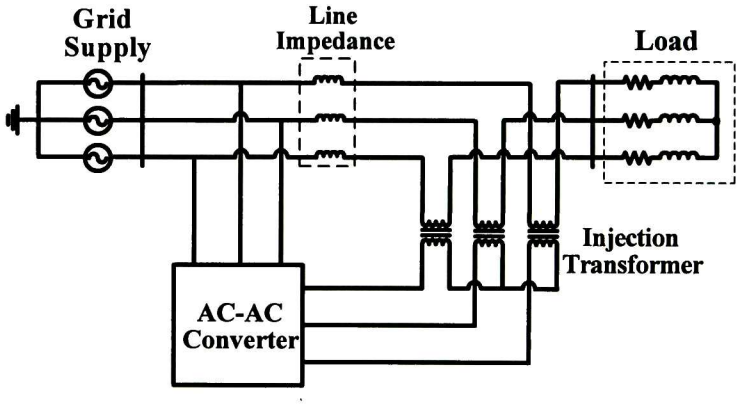

Figure 5.5. AC-AC DVR without energy storage devices.

The second type of configuration, Fig. 5.6, uses stored energy to feed the required power. DVR topologies with energy storage are highly favored to compensate deep level voltage sags to protect sensitive loads within a wide power factor range. However, as stated above a significant drawback relies on the overall system cost. In [5.8] and [5.9] a matrix converter-based DVR using flywheel energy storage is proposed for deep-level symmetric voltage sags. Considering that most of the voltage disturbances in distribution systems are asymmetric [5.13], the unbalanced voltage compensation function is a desirable operational characteristic for a practical DVR. In the same manner, since voltage sags generally only occur a few times each year at any particular location, a DVR system will generally spend most of its time in standby mode waiting for a sag to occur. Unfortunately, it will still introduce extra impedance to the line, primarily due to the series transformer and this impedance will in turn cause a voltage drop to the load and increased load voltage harmonics when non-linear loads are present [5.14]. In principle it would be advantageous if the series-connected inverter of the DVR could also be used to compensate for any steady state load voltage harmonics. This would increase the power quality benefits to the system, which is the definition and driving force of custom power systems, with minimal extra

capital cost, but of course, with some increase in inverter steady state losses. The limitations in achieving this objective could be steady state power flow constraints and the low modulation depths that must be used with a DVR that has a typical voltage injection capacity, but for ac-ac converter-based DVR it is still unclear.

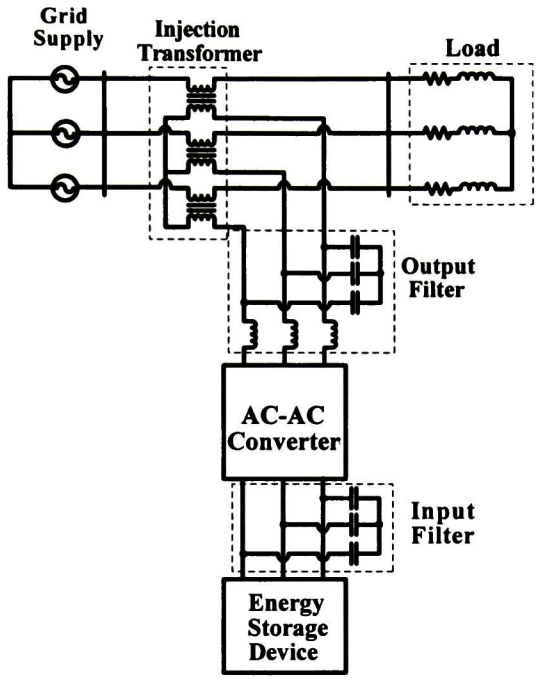

Figure 5.6. AC-AC DVR with energy storage device

Considering the previous aspects, a DVR topology should fulfill the next requirements:

- The device must have the ability to compensate deep-level symmetric voltage sags and unbalanced voltage variations.
- DVR system must provide voltage harmonic compensation capabilities with minimal effect o the sag compensation performance of the basic DVR.
- Minimization of cost and operational complexity.

Since in the case of no energy storage device configurations the energy is taken from the supply system in *ac* form, the best option for the line interface inverter is to employ an integrated ac-ac converter. Moreover, to accomplish asymmetric and harmonic voltage compensation, the ac-ac matrix converter operating with the modified SVM technique developed in chapter III, represents a very attractive solution, which leads to the proposed schemes in this dissertation. Compared to the existing DVR topologies, the herein proposed

topologies are developed according to the multi-functional requirements and are particularly tailored to the series compensation applications.

5.3 Matrix Converter-based DVR: Input Terminals Connected on the Supply Side (Topology 1)

The first DVR topology proposed, Fig 5.7, employs the matrix converter as the main device, and is developed with the purpose of compensate balance and unbalanced voltage variations as well as voltage harmonic distortion on the supply system voltages. Basically the proposed topology has the same structure as the one presented in Fig. 5.3a, the only difference is the substitution of the AC-DC-AC conversion arrangement by the ac-ac matrix converter. Since no energy storage device is used, the energy require for compensation is taken from the incoming supply. This approach has the disadvantage of drawing more current from the line during the fault, and hence the upstream loads will see a higher voltage drop. However, if the DVR is connected to a strong grid the necessary power to the load can be ensured by increasing the input current and injecting the missing voltage with the converter. Even when a saving is obtained on the energy storage system, the ability to compensate deep-level voltage sags is limited as the main disadvantage of matrix converter is the limited voltage transfer ratio.

During voltage sags, the input voltage of the matrix converter drops proportionally to the sag, hence the maximum injected voltage become,

$$\left|\overline{V}_{inj}\right| \approx \sqrt{3}/2 \cdot \left|\overline{a}\right| \tag{5.1}$$

where:
$\overline{V}_{inj}$ is the injected voltages in pu and $\overline{a}$ is a voltage sag factor defined as the ratio between the voltage during the sag and the load rated voltage.

For instance, if the supply falls to 0.5 pu at rated load, the maximum injection voltage generated by the matrix converter will be 0.432 pu, which would be unsatisfactory. Hence, the ability to compensate for symmetric voltage sags will be theoretically limited up to 0.45 pu voltage drops.

5.3.1 Modeling of the matrix converter DVR system

Figure 5.1 shows the schematic of the matrix converter-based DVR system for configuration 1. A second order LC filter is used at the input terminals of the converter to improve the input currents waveform. A second order RLC filter is utilized at the output

terminals of the matrix converter in order to filter the switching harmonic components in the generated voltages. The combined effect of the non ideal AC source and the three phase line is represented by the inductance Ls. The state equations for the ac quantities in the system can be formulated in synchronous reference frame in the complex vector domain. The state equations of the system can be consequently expressed using complex space vectors.

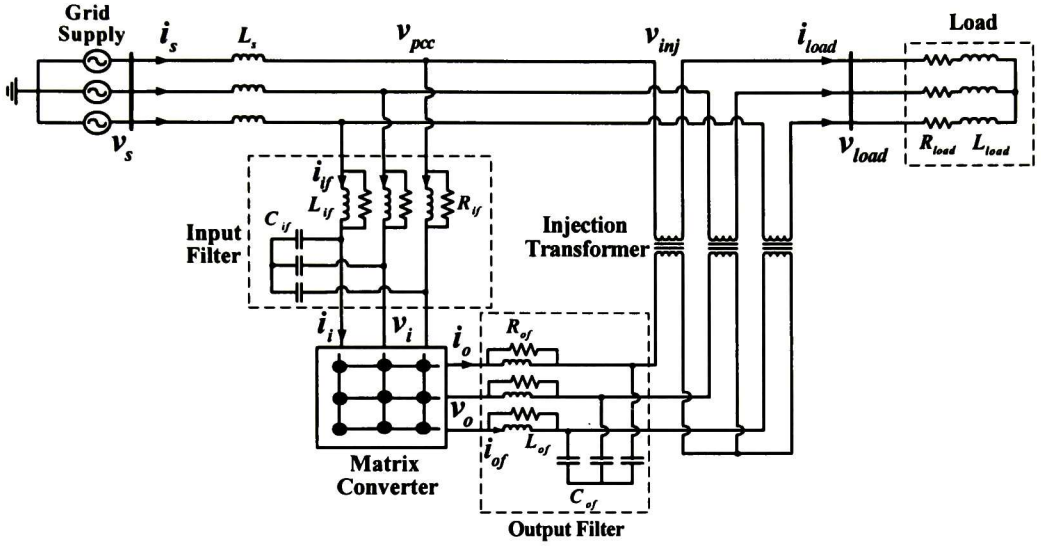

Figure 5.7. Proposed DVR with matrix converter input terminals connected on the supply side.

The dynamic behavior of the overall system can be established as follows.

- *Input Filter*

The dynamic equations for the input filter can be derived from the circuit law and they are given in (5.2).

$$\frac{di_{ds}}{dt} = \omega i_{qs} + \left(\frac{1}{L_s}\right)\left((v_{ds} - R_{if}(i_{ds} - i_{dif} - i_{dload}) - v_{di}\right)$$

$$\frac{di_{qs}}{dt} = -\omega i_{ds} + \left(\frac{1}{L_s}\right)\left((v_{qs} - R_{if}(i_{qs} - i_{qif} - i_{qload}) - v_{qi}\right)$$

$$\frac{di_{dif}}{dt} = \omega i_{qif} + \left(\frac{R_{if}}{L_{if}}\right)\left(i_{ds} - i_{dif} - i_{dload}\right) \qquad (5.2)$$

$$\frac{di_{qif}}{dt} = -\omega i_{dif} + \left(\frac{R_{if}}{L_{if}}\right)\left(i_{qs} - i_{qif} - i_{qload}\right)$$

$$\frac{dv_{di}}{dt} = \omega v_{qi} + \left(\frac{1}{C_{if}}\right)\left(i_{ds} - i_{dload} - i_{di}\right)$$

$$\frac{dv_{qi}}{dt} = -\omega v_{di} + \left(\frac{1}{C_{if}}\right)\left(i_{qs} - i_{qload} - i_{qi}\right)$$

- *Output filter*

Equations for the output filter are given by (5.3).

$$\begin{aligned}
\frac{di_{dof}}{dt} &= \omega i_{qof} + \frac{v_{do}}{L_{of}} - \frac{v_{dinj}}{L_{of}} \\
\frac{di_{qof}}{dt} &= -\omega i_{dof} + \frac{v_{qo}}{L_{of}} - \frac{v_{qinj}}{L_{of}} \\
\frac{dv_{dinj}}{dt} &= \omega v_{qinj} + \frac{i_{dof}}{C_{of}} + \frac{v_{do}}{R_{of}C_{of}} - \frac{v_{dinj}}{R_{of}C_{of}} - \frac{i_{dload}}{C_{of}} \\
\frac{dv_{qdinj}}{dt} &= -\omega v_{dinj} + \frac{i_{qof}}{C_{of}} + \frac{v_{qo}}{R_{of}C_{of}} - \frac{v_{qinj}}{R_{of}C_{of}} - \frac{i_{qload}}{C_{of}}
\end{aligned} \tag{5.3}$$

- *RC Load*

Considering an RC load, dynamic equations are given by (5.4).

$$\begin{aligned}
\frac{di_{dload}}{dt} &= \omega i_{qload} + \left(\frac{R_{if}}{L_{load}}\right)\left(i_{ds} - i_{dif} - i_{dload}\right) + \left(\frac{1}{L_{load}}\right)\left(v_{di} + v_{dinj}\right) - i_{dload}\left(\frac{R_{if} + R_{load}}{L_{load}}\right) \\
\frac{di_{qload}}{dt} &= -\omega i_{dload} + \left(\frac{R_{if}}{L_{load}}\right)\left(i_{qs} - i_{qif} - i_{qload}\right) + \left(\frac{1}{L_{load}}\right)\left(v_{qi} + v_{qinj}\right) - i_{qload}\left(\frac{R_{if} + R_{load}}{L_{load}}\right)
\end{aligned} \tag{5.4}$$

- *Matrix converter*

To establish the input/output voltage and current relationships of a matrix converter, the following assumptions are made [5.15]:

i) Power electronic switches are ideal
ii) Switching harmonics are neglected and only average voltage and currents over a switching period are considered.

Output phase voltages [v_A, v_B, v_C] are related to the input phase voltages [v_a, v_b, v_c] by,

$$[v_A \quad v_B \quad v_C]^T = M\,[v_a \quad v_b \quad v_c]^T \tag{5.5}$$

Transforming the three phase input and output voltages into their synchronous rotating reference frames yields:

$$\begin{bmatrix} v_{do} \\ v_{qo} \end{bmatrix} = M_{dq} \begin{bmatrix} v_{di} \\ v_{qi} \end{bmatrix} \tag{5.6}$$

Where v_{do} and v_{qo} are the d and q axis output voltages of the matrix converter; likewise, v_{di} and v_{qi} are the input voltages of the converter, all referred in the synchronous frame which rotates at an angular speed of ω.

For unity power factor the relationships between the input and output voltages can be further expressed by;

$$\begin{aligned} v_{do} &= (\sqrt{3} m V_{in} / 2)\cos\varphi_o \\ v_{do} &= -(\sqrt{3} m V_{in} / 2)\sin\varphi_o \end{aligned} \tag{5.7}$$

Where V_{in} is the peak input voltage, m is the modulation index and φ_o is the initial angle of the output voltage. Eq. (5.7) can be further reduced to,

$$\begin{aligned} v_{do} &= \frac{V_{in}}{U_i} v_{do} \\ v_{qo} &= \frac{V_{in}}{U_i} v_{qo} \end{aligned} \tag{5.8}$$

Where U_i is the peak voltage used by a modulation scheme to determine the modulation index m, and v_d^* and v_q^* are the demanded output voltages.

Using the duality principle, the d and q axis input currents of the matrix converter are related to the output currents by,

$$\begin{bmatrix} i_{di} \\ i_{qi} \end{bmatrix} = M_{dq}{}^T \begin{bmatrix} i_{do} \\ i_{qo} \end{bmatrix} \tag{5.9}$$

Which can be further reduced to, [5.15],

$$i_{di} = \frac{V_{di}}{U_i^2}\left(v_{do}^{*} i_{do} + v_{qo}^{*} i_{qo}\right) \tag{5.10}$$

$$i_{di} = \frac{V_{qi}}{U_i^2}\left(v_{do}^{*} i_{do} + v_{qo}^{*} i_{qo}\right)$$

The state-space equations for the complete matrix converter-based DVR system are:

$$\dot{\mathbf{X}} = \mathrm{f}(\mathbf{X}, \mathbf{U}) \tag{5.11}$$

where **X** and **U** are the vectors of the state variables and inputs respectively, and f(**X**,**U**) is the vector of the non-linear functions of **X** and **U**. They are given by:

$$\mathbf{X} = \begin{bmatrix} i_{ds} & i_{qs} & i_{dif} & i_{qif} & v_{di} & v_{qi} & i_{dof} & i_{qof} & v_{dinj} & v_{qinj} & i_{dload} & i_{qload} \end{bmatrix}^T;$$

$$\mathbf{U} = \begin{bmatrix} v_{ds} & v_{qs} & v_{do}^{*} & v_{qo}^{*} \end{bmatrix}^T;$$

$$f(\mathbf{X},\mathbf{U}) = \begin{bmatrix} f_1 & f_2 & f_3 & f_4 & f_5 & f_6 & f_7 & f_8 & f_9 & f_{10} & f_{11} & f_{12} \end{bmatrix}^T;$$

$$f_1 = \omega i_{qs} + \left(\frac{1}{L_s}\right)\left((v_{ds} - R_{if}(i_{ds} - i_{dif} - i_{dload}) - v_{di}\right)$$

$$f_2 = -\omega i_{ds} + \left(\frac{1}{L_s}\right)\left((v_{qs} - R_{if}(i_{qs} - i_{qif} - i_{qload}) - v_{qi}\right)$$

$$f_3 = \omega i_{qif} + \left(\frac{R_{if}}{L_{if}}\right)\left(i_{ds} - i_{dif} - i_{dload}\right)$$

$$f_4 = -\omega i_{dif} + \left(\frac{R_{if}}{L_{if}}\right)\left(i_{qs} - i_{qif} - i_{qload}\right)$$

$$f_5 = \omega v_{qi} + \left(\frac{1}{C_{if}}\right)\left(i_{ds} - i_{dload} - \frac{v_{di}}{U_i^2}\left[v_{do}^{*}\left(i_{dof} + \frac{V_{in}}{U_i R_{of}} v_{do}^{*} - \frac{v_{dinj}}{R_{of}}\right) + v_{qo}^{*}\left(i_{qof} + \frac{V_{in}}{U_i R_{of}} v_{qo}^{*} - \frac{v_{qinj}}{R_{of}}\right)\right]\right)$$

$$f_6 = -\omega v_{di} + \left(\frac{1}{C_{if}}\right)\left(i_{qs} - i_{qload} - \frac{v_{qi}}{U_i^2}\left[v_{qo}^{*}\left(i_{qof} + \frac{V_{in}}{U_i R_{of}} v_{qo}^{*} - \frac{v_{qinj}}{R_{of}}\right) + v_{do}^{*}\left(i_{dof} + \frac{V_{in}}{U_i R_{of}} v_{do}^{*} - \frac{v_{dinj}}{R_{of}}\right)\right]\right)$$

$$f_7 = \omega i_{qof} + \frac{1}{L_{of}}\left(\frac{V_{in}}{U_i} v_{do}^{*}\right) - \frac{v_{dinj}}{L_{of}}$$

$$f_8 = -\omega i_{dof} + \frac{1}{L_{of}}\left(\frac{V_{in}}{U_i} v_{qo}^{*}\right) - \frac{v_{qinj}}{L_{of}}$$

$$f_9 = \omega v_{qinj} + \frac{i_{dof}}{C_{of}} + \frac{1}{R_{of} C_{of}}\left(\frac{V_{in}}{U_i} v_{do}^{*}\right) - \frac{v_{dinj}}{R_{of} C_{of}} - \frac{i_{dload}}{C_{of}}$$

$$f_{10} = -\omega v_{dinj} + \frac{i_{qof}}{C_{of}} + \frac{1}{R_{of} C_{of}}\left(\frac{V_{in}}{U_i} v_{qo}^{*}\right) - \frac{v_{qinj}}{R_{of} C_{of}} - \frac{i_{qload}}{C_{of}}$$

$$f_{11} = \omega i_{qload} + \left(\frac{R_{if}}{L_{load}}\right)\left(i_{ds} - i_{dif} - i_{dload}\right) + \left(\frac{1}{L_{load}}\right)\left(v_{di} + v_{dinj}\right) - i_{dload}\left(\frac{R_{if} + R_{load}}{L_{load}}\right)$$

$$f_{12} = -\omega i_{dload} + \left(\frac{R_{if}}{L_{load}}\right)\left(i_{qs} - i_{qif} - i_{qload}\right) + \left(\frac{1}{L_{load}}\right)\left(v_{qi} + v_{qinj}\right) - i_{qload}\left(\frac{R_{if} + R_{load}}{L_{load}}\right)$$

where, $V_{im} = \sqrt{v_{di}^2 + v_{qi}^2}$

5.3.2 DVR controller

The objective of the DVR controller is to control the load voltages through the injection of the right compensation voltages, ensuring a good transient response. Two control methods may generally be used for DVRs, being either open-loop control, or closed-loop control. A control structure fulfilling this objective is shown in Fig. 5.8. The primary control structure is based on a combination of supply voltage feed-forward and a PI-based load voltage feed-back. The feed-forward component provides the required transient response at the beginning of the disturbance and reduces the overvoltage caused at system restoration. However, it does not account for the voltage drop across the filter inductor and other parameters such as the transformer. Therefore, a closed-loop load voltage feedback is added, and is implemented in the d-q frame to minimize any steady state error in the fundamental component.

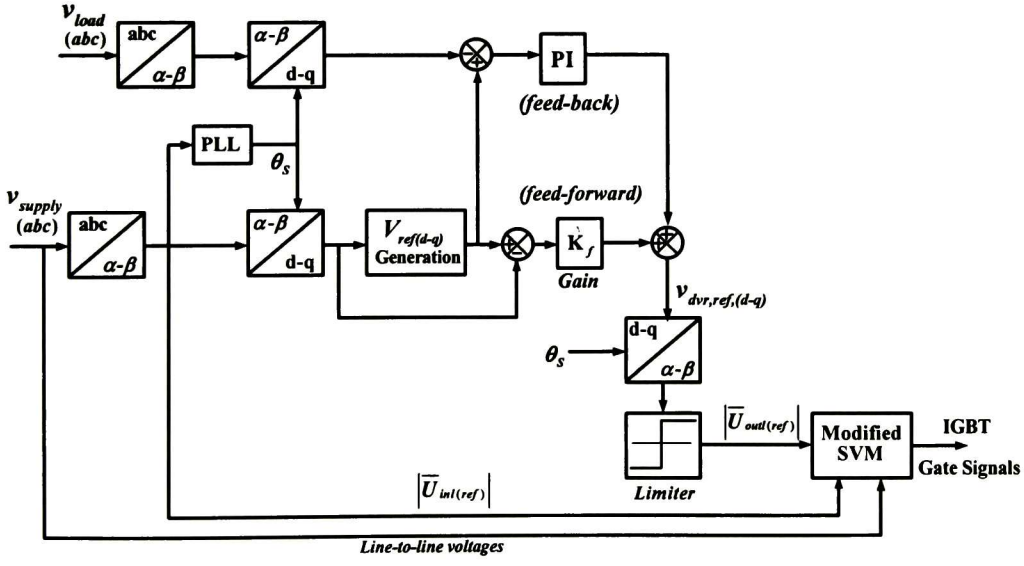

Figure 5.8. Proposed DVR control scheme

The DVR is synchronized to the grid supply with a phase-locked loop (PLL). A relatively slow PLL is used to limit influence from harmonics and non-symmetrical input voltages and also to maintain a smooth output voltage even during the phase jump presented during the disturbance [5.4],[5.16]. When a disturbance occurs, the PLL reacts slowly and consequently the phase variation is minimum compared to the pre-sag condition. In this way the PLL allows synchronization during the compensation process.

As shown in Fig. 5.8, the voltage at PCC, v_{pcc}, is measured and transformed to a rotating dq reference frame. The actual state of the supply voltages $v_{pcc(d-q)}$ is used for voltage disturbance detection and for load voltage reference generation. After a disturbance is detected, the difference between the voltage reference $v_{ref(d-q)}$ and measured voltage $v_{pcc(d-q)}$ is utilized to determine the reference DVR injection voltage. Considering a coupling transformer with a unity voltage ratio, the DVR injected voltages would be approximately the matrix converter output voltages.

The transformed load voltage $v_{load(d-q)}$ is compared with the voltage reference $v_{ref(d-q)}$ and the error is fed to a PI-based voltage controller. Outputs from both main control ranches are combined to generate the compensation references to the DVR, $v_{dvr,ref(d-q)}$, which are then transformed into $\alpha\beta$ coordinates in order to implement the modified SVM technique. In the modulation technique proposed for controlling the matrix converter, the main control variables are $\left|\overline{U}_{outl(ref)}\right|$ and $\left|\overline{U}_{inl}\right|$ corresponding to the magnitudes of the DVR injected voltage reference and the supply system voltage Park vectors, respectively. The limiter block in the controller is employed to avoid DVR false operations. The modified SVM scheme incorporates the characteristics of the supply voltages into the computation of the duty cycles. The only restriction that needs to be verified in the modulation scheme proposed is established by eq. (5.12).

$$\left|\overline{U}_{outl(ref)}\right| < \sqrt{3}/2 \left|\overline{U}_{inl}\right| \tag{5.12}$$

5.4 Matrix Converter-based DVR: Input Terminals Connected on the Load Side (Topology 2)

The second DVR topology proposed, Fig 5.9, is based on the dc-link configuration with a no energy storage device and a shunt converter connected on the load side, Fig. 5.3b. As was established in previous sections, this topology is good alternative for voltage compensation due to its good performance and relatively low cost. However, the negative grid effects caused by the distorted current drawn by the shunt converter could disqualify this solution for certain applications.

It is well known that one of the most attractive advantages of matrix converter is the quality of the input current signals. This characteristic leads to the second proposed scheme in this dissertation. By including an integrated ac-ac converter instead of the conventional *ac-dc-ac* structure, the negative grid effects associated with this topology can be reduced. Furthermore, with this topology the voltage on the matrix converter input terminals can be held almost constant at the load rated level by injecting sufficient voltage which increases DVR compensation capability. So,

$$\left|\overline{V}_i\right| \approx \left|\overline{V}_{load}\right| \approx \left|\overline{V}_s + \overline{V}_{inj}\right| \tag{5.13}$$

where:

$\left|\overline{V}_i\right|$ = Matrix converter input voltages

$\left|\overline{V}_{load}\right|$ = Load voltages

$\left|\overline{V}_s\right|$ = System voltages

$\left|\overline{V}_{inj}\right|$ = Injected voltages

To exemplify the operation of the DVR with proposed configuration 2, it will be consider that the supply voltage falls to 0.5 pu at rated load. In this condition the matrix converter can generates a maximum voltage of 0.433 pu. Then, the load voltage would be 0.933 as well as the voltage available at the matrix converter input terminals. The compensation can be seen as an accumulative process in which as long as the matrix converter keeps injecting voltage, the available voltage for compensation grows until the load reaches its rated value. In this way, this topology overcomes the matrix converter limited voltage ratio disadvantage the only drawback is that the converter has to handled large currents.

5.4.1 Modeling of the matrix converter DVR system

Figure 5.9 shows the schematic of the matrix converter-based DVR system for configuration 2. A second order RLC filter is used at the input terminals of the converter to improve the input currents waveform. A second order LC filter is utilized at the output terminals of the matrix converter in order to filter the switching harmonic components in the generated voltages. The state equations of the system in the synchronous reference frame are expressed as follows.

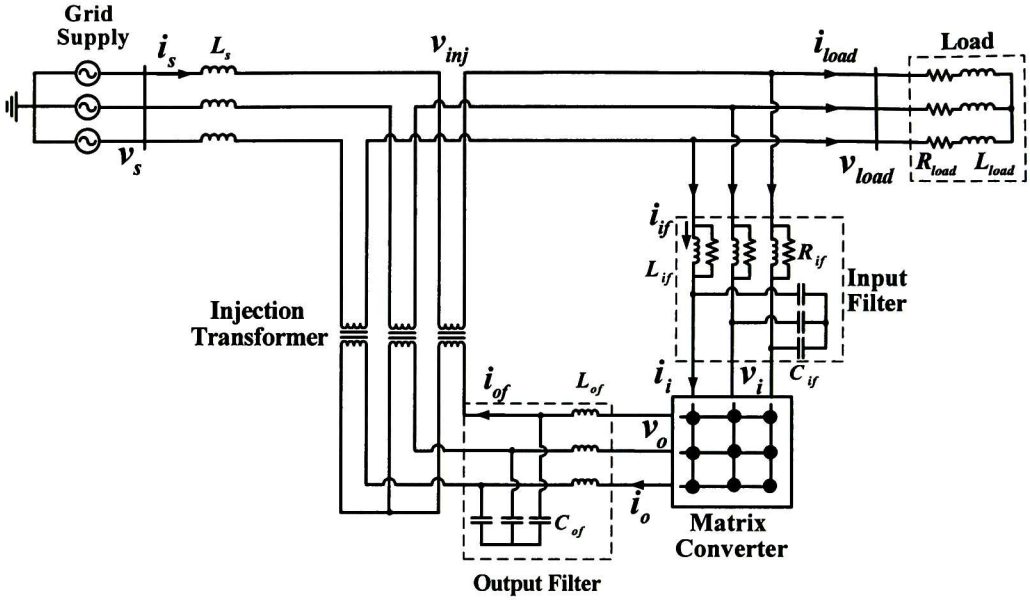

Figure 5.9. Proposed DVR with matrix converter input terminals connected on the load side.

- *Input Filter*

Equations for the input filter are given by (5.14).

$$\begin{aligned}
\frac{di_{dif}}{dt} &= \omega i_{qif} + \left(\frac{1}{L_{if}}\right)\left(v_{ds} + v_{dinj} - v_{di}\right) \\
\frac{di_{qif}}{dt} &= -\omega i_{dif} + \left(\frac{1}{L_{if}}\right)\left(v_{qs} + v_{qinj} - v_{qi}\right) \\
\frac{dv_{di}}{dt} &= \omega v_{qi} + \frac{i_{dif}}{C_{if}} + \frac{1}{C_{if}R_{if}}\left(v_{di} - v_{ds} + v_{dinj}\right) \\
\frac{dv_{qi}}{dt} &= -\omega v_{di} + \frac{i_{qif}}{C_{if}} + \frac{1}{C_{if}R_{if}}\left(v_{qi} - v_{qs} + v_{qinj}\right)
\end{aligned} \tag{5.14}$$

- *Output filter*

Equations for the output filter are given by (5.15).

$$\frac{di_{do}}{dt} = \omega i_{qo} + \frac{1}{L_{of}}\left(v_{do} - v_{dinj}\right)$$

$$\frac{di_{qo}}{dt} = -\omega i_{do} + \frac{1}{L_{of}}\left(v_{qo} - v_{qinj}\right)$$
$$\frac{dv_{dinj}}{dt} = \omega v_{qinj} + \frac{1}{C_{of}}\left(i_{do} + i_{ds}\right) \tag{5.15}$$
$$\frac{dv_{qinj}}{dt} = -\omega v_{dinj} + \frac{1}{C_{of}}\left(i_{qo} + i_{qs}\right)$$
$$\frac{di_{ds}}{dt} = \omega v_{qs} + \frac{1}{L_s}\left(v_{ds} + v_{dinj}\right)$$
$$\frac{di_{qs}}{dt} = -\omega v_{ds} + \frac{1}{L_s}\left(v_{qs} + v_{qinj}\right)$$

- *RC Load*

Considering an RC load, dynamic equations are given by (5.16).

$$\frac{di_{dload}}{dt} = \omega i_{qload} + \left(\frac{1}{L_{load}}\right)\left(v_{ds} + v_{dinj} - R_{load} \cdot i_{dload}\right) \tag{5.16}$$
$$\frac{di_{qload}}{dt} = -\omega i_{dload} + \left(\frac{1}{L_{load}}\right)\left(v_{qs} + v_{qinj} - R_{load} \cdot i_{qload}\right)$$

- *Matrix converter*

Input/output voltage and current relationships of a matrix converter were established in section 5.4.1. Taking into account eqs., (5.8) and (5.10), the state-space equations for the complete matrix converter-based DVR system are:

$$\dot{\mathbf{X}} = \mathrm{f}(\mathbf{X}, \mathbf{U}) \tag{5.17}$$

where **X** and **U** are the vectors of the state variables and inputs respectively. f(**X**,**U**) is the vector of the non-linear functions of **X** and **U**. They are given by:

$$\mathbf{X} = \left[i_{ds} \quad i_{qs} \quad i_{dif} \quad i_{qif} \quad v_{di} \quad v_{qi} \quad i_{do} \quad i_{qo} \quad v_{dinj} \quad v_{qinj} \quad i_{dload} \quad i_{qload}\right]^T;$$
$$\mathbf{U} = \left[v_{ds} \quad v_{qs} \quad v_{do}^{*} \quad v_{qo}^{*}\right]^T;$$
$$f(\mathbf{X},\mathbf{U}) = \left[f_1 \quad f_2 \quad f_3 \quad f_4 \quad f_5 \quad f_6 \quad f_7 \quad f_8 \quad f_9 \quad f_{10} \quad f_{11} \quad f_{12}\right]^T;$$

$$f_1 = \omega v_{qs} + \frac{1}{L_s}\left(v_{ds} + v_{dinj}\right)$$

$$f_2 = -\omega v_{ds} + \frac{1}{L_s}\left(v_{qs} + v_{qinj}\right)$$

$$f_3 = \omega i_{qif} + \left(\frac{1}{L_{if}}\right)\left(v_{ds} + v_{dinj} - v_{di}\right)$$

$$f_4 = -\omega i_{dif} + \left(\frac{1}{L_{if}}\right)\left(v_{qs} + v_{qinj} - v_{qi}\right)$$

$$f_5 = \omega v_{qi} + \frac{i_{dif}}{C_{if}} + \frac{1}{C_{if}R_{if}}\left(v_{di} - v_{ds} + v_{dinj}\right)$$

$$f_6 = -\omega v_{di} + \frac{i_{qif}}{C_{if}} + \frac{1}{C_{if}R_{if}}\left(v_{qi} - v_{qs} + v_{qinj}\right)$$

$$f_1 = \omega i_{qo} + \frac{1}{L_{of}}\left(\frac{V_{in}}{U_i}v_{do}^{*} - v_{dinj}\right)$$

$$f_2 = -\omega i_{do} + \frac{1}{L_{of}}\left(\frac{V_{in}}{U_i}v_{qo}^{*} - v_{qinj}\right)$$

$$f_9 = \omega v_{qinj} + \frac{1}{C_{of}}\left(i_{do} + i_{ds}\right)$$

$$f_{10} = -\omega v_{dinj} + \frac{1}{C_{of}}\left(i_{qo} + i_{qs}\right)$$

$$f_{11} = \omega i_{qload} + \left(\frac{1}{L_{load}}\right)\left(v_{ds} + v_{dinj} - R_{load} \cdot i_{dload}\right)$$

$$f_{12} = -\omega i_{dload} + \left(\frac{1}{L_{load}}\right)\left(v_{qs} + v_{qinj} - R_{load} \cdot i_{qload}\right)$$

where, $V_{im} = \sqrt{v_{di}^2 + v_{qi}^2}$

5.4.2 DVR controller

In the proposed DVR topology 2, a controller very similar to the one analyzed in section 5.4.2, is utilized. As can be seen in Fig. 5.10, the only difference between both controllers is in the way they obtain the magnitude $|\overline{U}_{inl}|$ corresponding to the matrix converter input voltage and which represents the voltage available for compensation. Since in this topology the input terminals of the converter are connected on the load side of the system, the input voltage magnitude should correspond to the load voltages. However, by utilizing the voltage reference in the $\alpha\beta$ coordinates, the DVR response is more stable.

This strategy can be seen as a predictive control in which the controller is always fed with the ideal condition, $|\overline{U}_{inl}| = v_{load} = 1$ pu and sinusoidal. In this manner, the distortion

presented in the actual input voltages at the moment the disturbance occurs does not affect the compensation-voltage generation. A remarkable transient response is accomplished by adjusting the gain on the feed-forward control branch, as well as the proportional and integral gains of the PI controller.

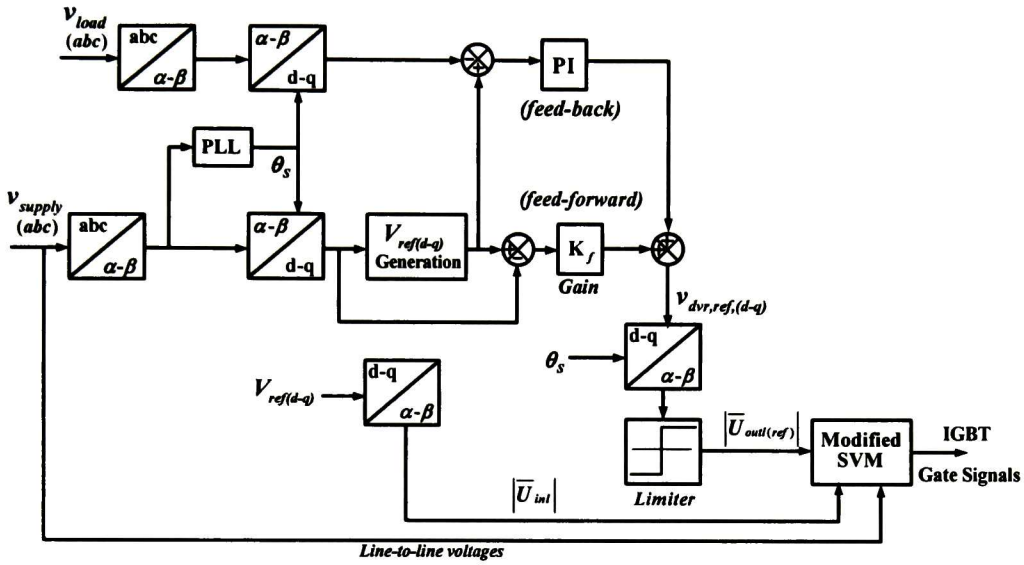

Figure 5.10. Proposed DVR configuration 2 control scheme

5.5 Conclusions

In this chapter two novel DVR topologies based on the matrix converter have been proposed. At first, the conventional DVR configuration was evaluated, concluding that the main drawbacks of this topology reside in the DC-link and the way the energy required for it is obtained. Then, existing DVR topologies were evaluated and the ones with AC-AC power conversion and no energy storage were selected based on the evaluation of each topology and the objectives planned at the beginning of the research. Both proposed topologies have been analyzed and mathematical models have been obtained, aimed to future stability analysis.

Finally a voltage controller, based on a PI controller, was designed with the objective of get a fast dynamic response. The controller has a combination of feed-back and feed-forward schemes to improve the overall response of the system.

The incorporation of the matrix converter technology to the voltage compensation devices is intended to reduce the cost and size of power converters commonly used while improves the reliability.

5.6 References

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CHAPTER VI

Simulation and Experimental Results

This chapter presents implementation details of the matrix converter laboratory prototype analyzed in previous chapters. This prototype will be used to validate the performance of the two DVR topologies proposed.

In order to establish the capabilities of the DVR, simulation results through detailed dynamic models implemented in PSCAD software, are presented. Experimental results are also provided for both DVR topologies.

6.1 Matrix Converter Prototype

As already presented in previous chapters, the matrix converter needs certain elements in order to run properly. A low pass filter at the input terminals is used to reduce the high frequency ripple from the input current. A clamp circuit, which consists of a capacitor and two B6 diode bridges in a back-to-back configuration connected to the input and output lines, to protect the converter against over-voltages in both sides.

For a proper analysis of the matrix converter prototype performance, aspects related to unavailability of various desirable components have to be taken into account.

6.1.1 Matrix of bidirectional switches

An important drawback of building a matrix converter prototype is the lack of power semiconductor bi-directional switches. When such devices are developed in a reduced number for research purpose, these are more expensive than regular devices at equivalent ratings, which mean that is very expensive to start building custom designed devices for a wide power range. Therefore, the construction of a low voltage prototype was decide for

this research, in order to obtained representative results just to validate the DVR configurations proposed in the dissertation.

For the bidirectional switches a common emitter configuration was adopted, as indicated in Fig 6.1. Due to the unavailability of a power module that integrates the set of bidirectional switches, the matrix converter power stage was built with analog devices. For building the bidirectional switches the 12N60A4D IGBT was used, along with the integrated driver and opto-coupler HCPL-3120. The common-emitter requires nine isolated DC sources for supply the power cells, in this case were implemented with AM1S-0515SZ DC-DC converters.

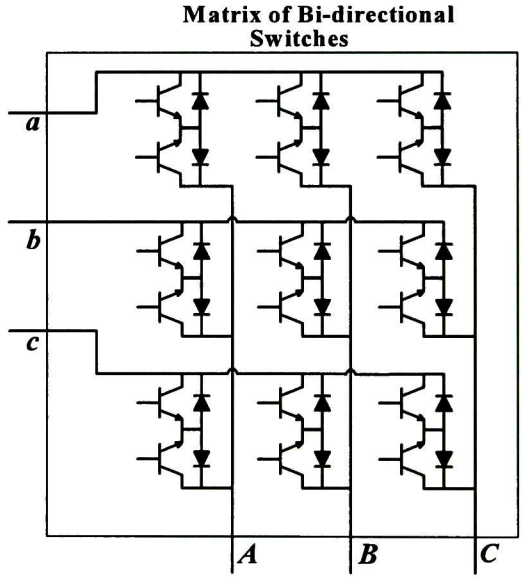


Figure 6.1. Matrix converter structure with IGBT's in common-emitter configuration

The PCB layout, which includes the nine bi-directional switches and the nine isolated DC sources, is displayed in Fig. 6.2. It is clear to see from Fig. 6.2, that some of the connection paths between IGBTs from the same bidirectional cell are quite long, resulting in significant stray inductances which causes internal over-voltages and limit the power capacity of the overall converter. Fig. 6.3 presents the matrix converter physical arrangement.

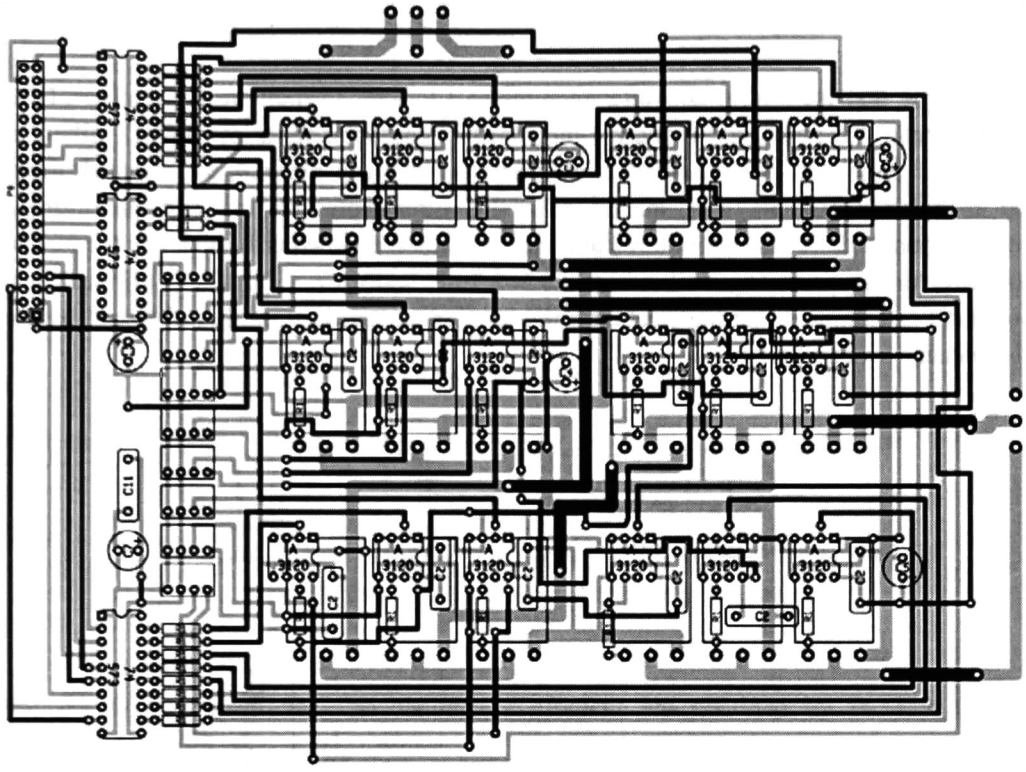


Figure 6.2. Matrix converter PCB layout

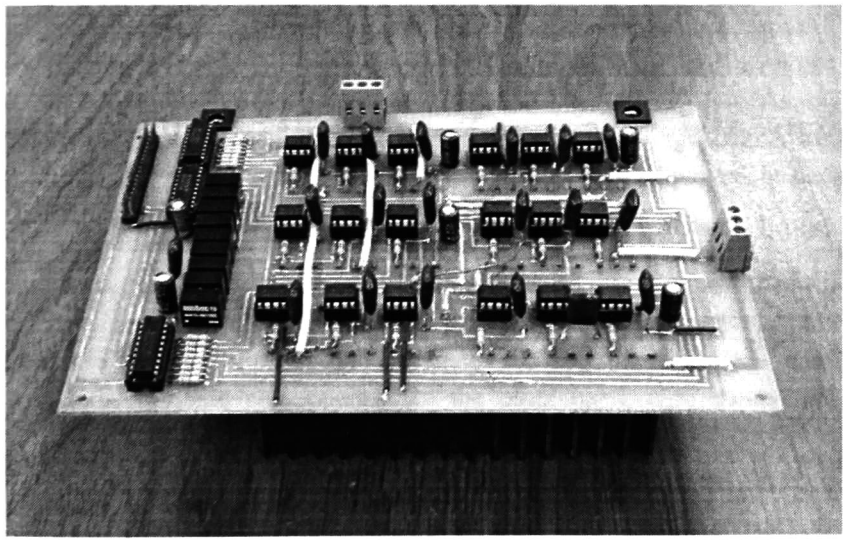


Figure 6.3. Matrix converter Prototype

6.1.2 The input filter

Considering that the matrix converter requires an LC filter to improve the quality of the input current, it is necessary to analyze the possible topologies for a low pass LC filter. In [6.1] a comparison of the LC filters configurations exhibit in Fig. 6.4, is presented. From the analysis exposed in [6.1], the one-stage LC filter represents the best commitment between number of elements required and the attenuation degree performed. For the matrix converter prototype an input filter with L_{if} = 2.2mH and a C_{if} = 10 μF, is utilized. It is important to comment that the election of the element values is strongly influenced by the components availability.

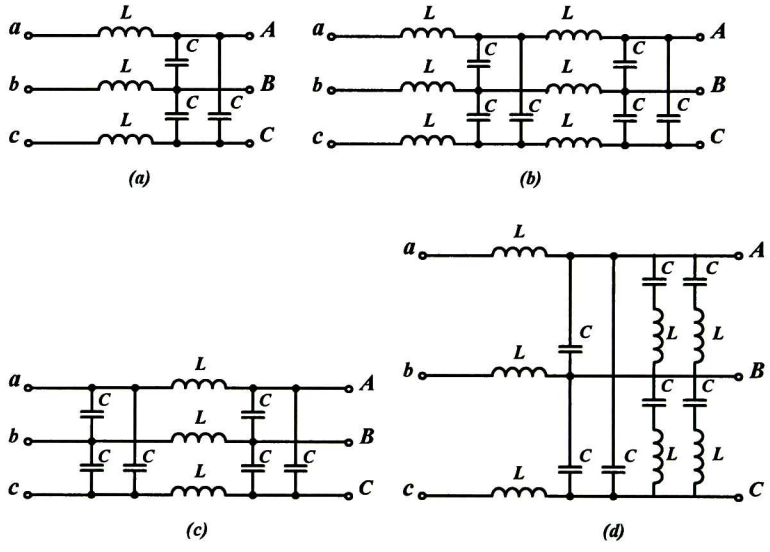


Figure 6.4. LC Filter configurations. a) One-stage LC filter, b) Multi-stage LC filter, c) π LC filter, and d) One-stage LC filter with notch addition.

Thus, the cut-off frequency of the filter can be obtained by,

$$f_o = \frac{1}{2\pi\sqrt{L_{if} \cdot C_{if}}} = \frac{1}{2\pi\sqrt{(2.2x10^{-3})(10x10^{-6})}} = 1.073kHz \tag{6.1}$$

With the one-stage LC filter the gain at resonance frequency is high enough to deteriorate the quality of the current waveform. With the purpose of reduce this effect is necessary to implement a damping circuit as the one represented in Fig. 6.5. This topology also improves the system stability [6.2], therefore is the one selected for the matrix converter prototype.

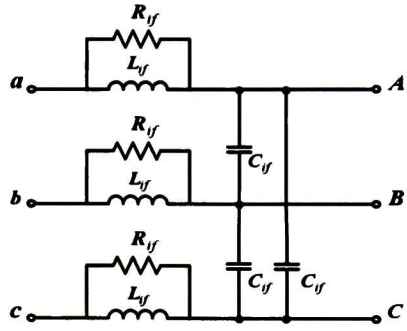


Figure 6.5. L-C filter with the addition of a damping resistor

The transfer function of the input filter is given by,

$$H(s) = \frac{1 + \frac{L_{if}}{R_{if}} s}{1 + \frac{L_{if}}{R_{if}} s + C_{if} L_{if} s^2} \tag{6.2}$$

The cut-off frequency and the damping coefficient are obtained by (6.1) and (6.3) respectively.

$$\xi = \frac{1}{2R_{if}} \sqrt{\frac{L_{if}}{C_{if}}} \tag{6.3}$$

Figure 6.6 illustrates the LC filter's frequency response with and without damping resistance. The addition of the damping resistance to the filter reduces considerably the gain at the resonance frequency; even though the attenuation degree is reduced as well. A 50Ω resistance was used for simulating tests while the 13.3Ω was employed in experimental implementation.

Input current waveforms with different input filter conditions are presented in Fig. 6.7. As Figure 6.7 illustrates, using the LC filter without damping resistor reduces the harmonic content around switching frequency but introduces some harmonics of low order, mainly the 18^{th} and 19^{th} harmonic components. On the other hand, with the addition of the damping resistor the low order harmonics are eliminated but some harmonics around switching frequency still remains, although with considerably reduced magnitudes. Last filter configuration was considered in both DVR topologies.

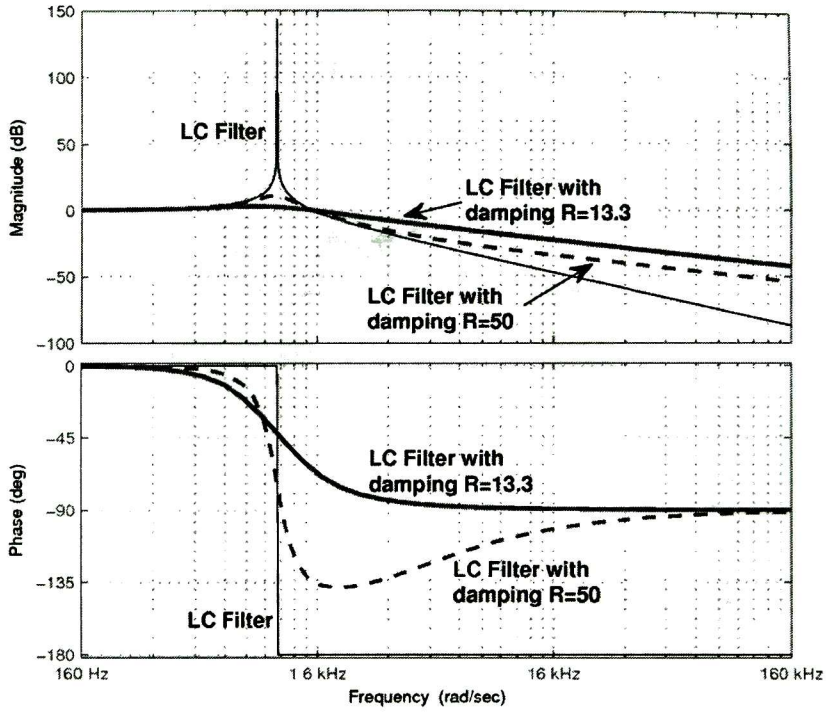


Figure 6.6. Frequency response of LC filter with and without damping resistor (L=2.2 mH, C= 10μF, R = 13.3 Ω, R=50Ω). Top: Magnitude response. Bottom: Phase response

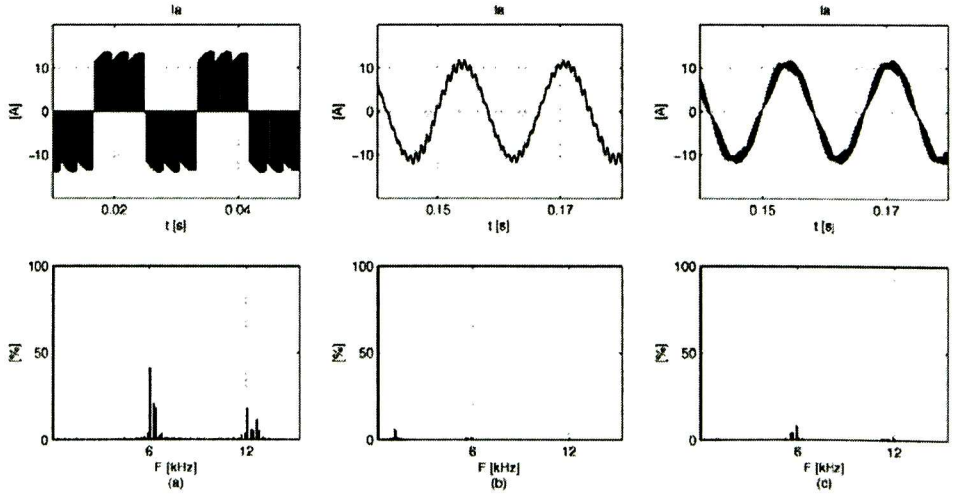


Figure 6.7. Harmonic analysis of matrix converter phase *a* input current made with PSCAD software. a) Without filter, b) With One-stage LC filter, c) With One-stage LC filter with damping resistor (R=13.3Ω).

6.1.3 The control system

Aimed to provide high performance results, the control strategy of the matrix converter was implemented in the Texas Instruments DSP board eZdsp-TMS320F2812, programmed in C language through the Code Composer Studio development environment (simulator, compiler and programmer).

Figure 6.8 shows the cyclic task operation of the control system. The core of the system is the DSP which produces all signals necessary for the control, including the signals required in the commutation logic for the four-step commutation strategy. Since the selected IGBTs have a turn on time of 17 ns and a turn off time of 96 ns, the signals exhibit in Fig. 6.9 are generated in order to achieve the proper four-step commutation operation. Timer T2 is configured to run in the automatic reload mode at a 6 kHz rate. The order in which the signals to control the matrix converter switches are generated is as follows:

- Timer T2 overflow triggers the ADC every 166 μs. The ADC performs nine conversions, three input voltage signals, three output voltage signals and the three signals of the output current signs. After the signals are read and stored in ADC registers, the ADC triggers a user-defined interruption.
- The code inside the interruption performs SVM control. First, matrix converter duty cycles are computed and loaded in the corresponding variables. Then, the new switching states are calculated using a look-up table that stores the 21 permitted commutation states.
- Timer T1 is configured in period match mode to count for duty cycle duration. Every time that T1 matches the value stored in the corresponding register for the period, an interruption is triggered. The code in that interruption reloads the new switching state and new duty cycle.

The procedure explained above repeats every switching period producing the switching pattern for the MDSVM strategy revised in chapter IV. The task of the DSP which performs the matrix converter control is shown in Fig. 6.10, and these are:

- Starts acquisitions of the three input voltages, the three output voltages and the three output current signs.
- Performs output voltage reference vector calculation
- Performs input current reference vector calculation
- Performs reference vectors tracking
- Calculates the modulation indexes for the modified SVM strategy proposed
- Calculates the commutation sequence
- Performs four-step commutation strategy.

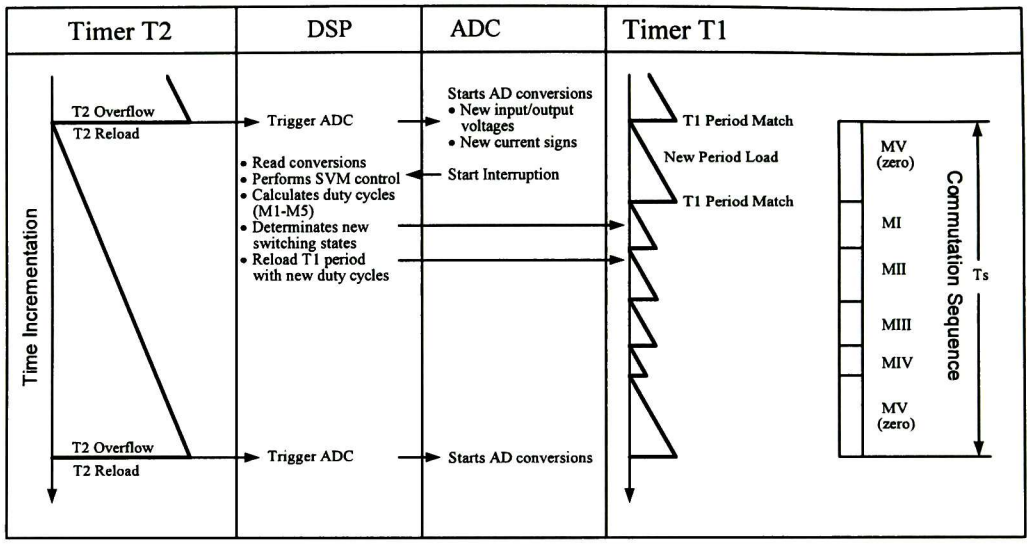
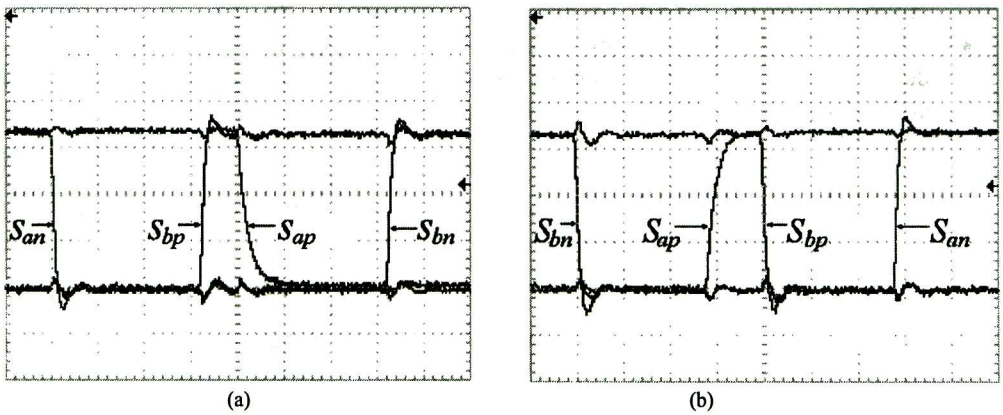


Figure 6.8. Control system task management of the matrix converter prototype



(a) (b)

Figure 6.9. Signals generated by the DSP on the four step commutation strategy. (a) Commutation from phase *a* to phase *b*. b) Commutation from phase *b* to phase *a*. (1V/div, 100ns/div).

Among the two DVR configurations proposed, the only difference regarding the control scheme of Fig. 6.10 is found on the generation of vector $\overline{U}_{inl}$. For topology 1, vector $\overline{U}_{inl}$ is generated from the input voltages whereas in topology 2 the same vector is generated from the reference voltage, as indicated by dotted lines.

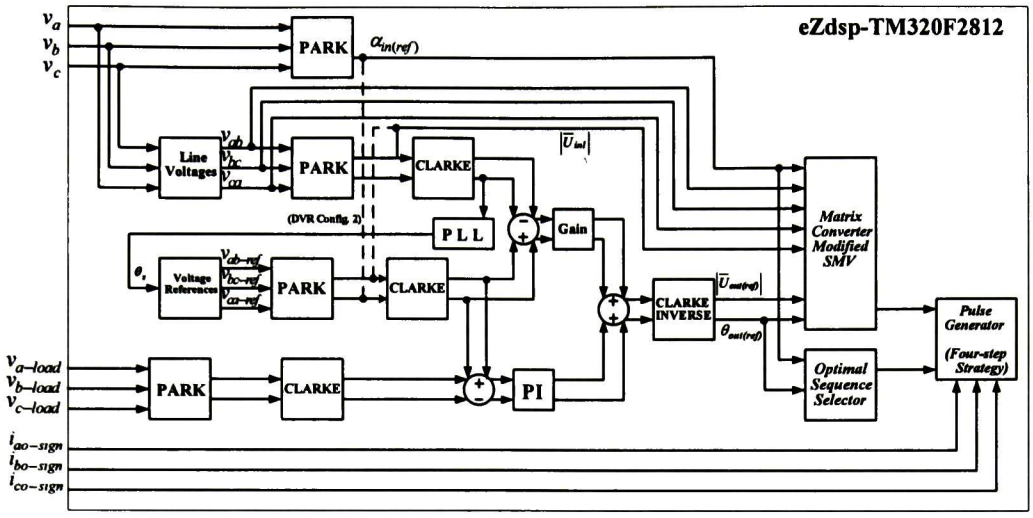


Figure. 6.10. DSP control diagram for the matrix converter prototype

6.2 DVR Topology 1 Results

The performance of the whole DVR system is verified by detailed numerical simulation using PSCAD software and through experimental tests. The system key parameters for the simulations are given in Table 6.1. The DVR topology 1 matrix converter-based, Fig. 6.11, is used for asymmetric voltage sags and swells compensation, as well as a voltage harmonics filtering. For improving injected voltage's quality, a RLC output filter is utilized.

6.2.1 Numerical verification

In the first study case an unbalanced disturbance is applied in the supply system, consisting of a voltage sag of 40% over input phase *b*. The Parks' vectors $\overline{U}_{inl}$ and $\overline{U}_{outl}$ on the complex plane are displayed in Fig. 6.12. In this case, voltage imbalance is exhibited on both set of terminals in the matrix converter. Nonetheless, as long as the vector $\overline{U}_{outl}$ remains inside the vector $\overline{U}_{inl}$ loci, the control algorithm is able to synthesize the compensation voltages. Figs. 6.13 and 6.14 depict selected voltage and current waveforms during voltage sag period (from 0.4 s until 0.5 s).

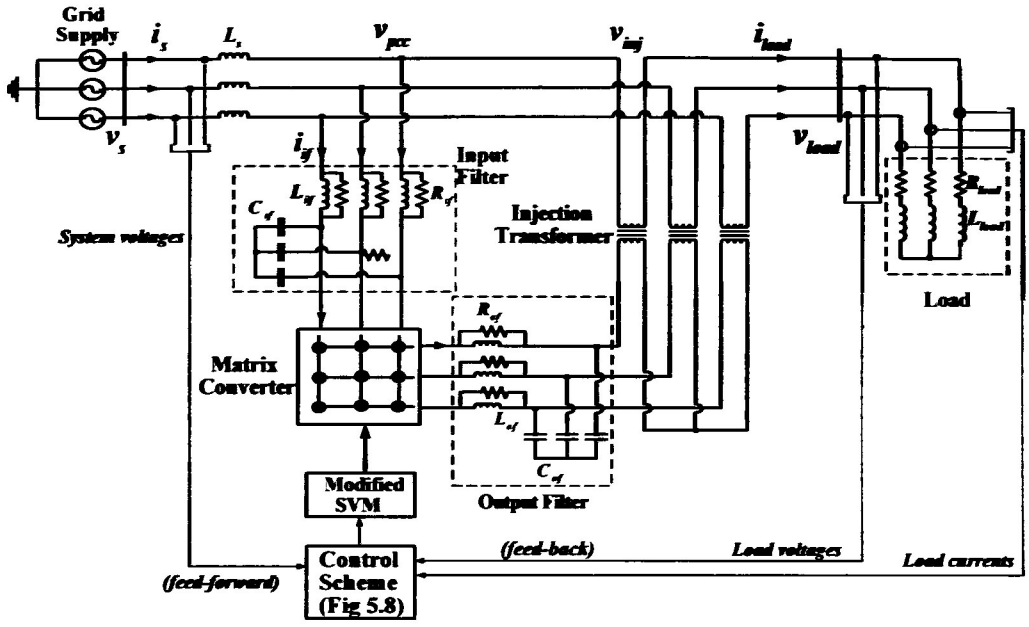


Figure 6.11. Proposed DVR topology 1 system architecture

Table 6.1 System Parameters

Parameter	Value
C_{if}: Input filter capacitor	10 μF
L_{if}: Input filter inductor	2.1 mH
R_{if}: Input filter resistor	50 Ω
C_{of}: Output filter capacitor	4.7 μF
L_{of}: Output filter inductor	25 mH
R_{of}: Output filter resistor	100 Ω
L_{load}: Load Inductor	213 mH
R_{load}: Load Resistor	120 Ω

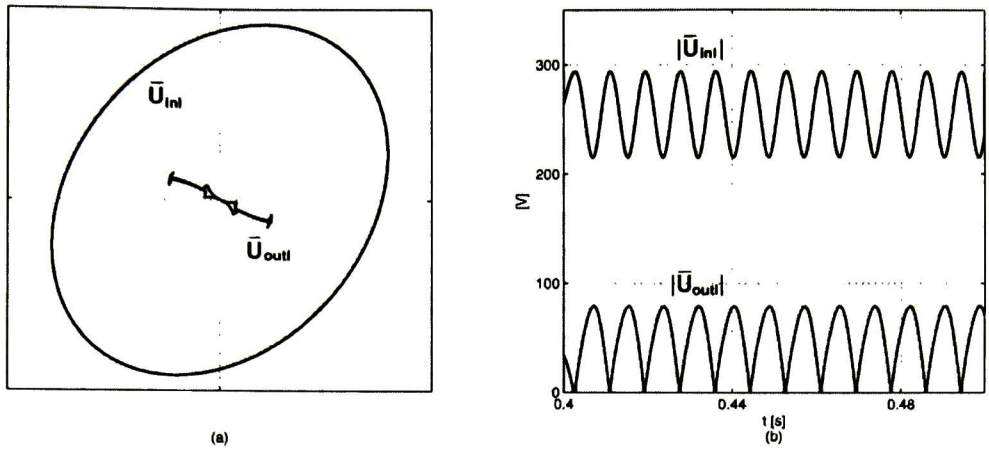


Figure 6.12. a). $\overline{U}_{inl}$ and $\overline{U}_{outl}$ in the complex space. b) Vectors magnitude

The control algorithm has accomplished to reduce the imbalanced percent from 15.38% at the input voltages to 0.42%, value which fulfils the NEMA criterion about permitted imbalance percent of 1%. Besides, each phase output voltage presents an average THD less than 3% during the fault which falls inside the guidelines established in the IEEE-519 for general power systems of medium voltage.

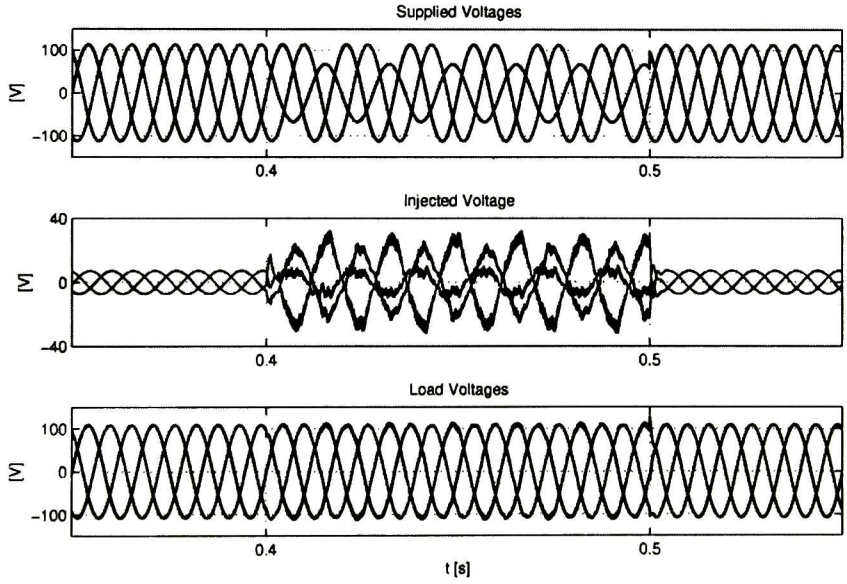


Figure 6.13. DVR response under unbalanced voltage variation. From top to bottom: Supply voltages, injected voltages and load voltages

In Fig. 6.14, the shown output-currents do not exhibit any variation during the disturbance. The RL load acts as a low-pass filter reducing almost all the harmonic components, as can be seen in the figure. On the other hand, the matrix converter generates a set of unbalanced voltages to achieve the compensation, which provokes a distortion in the currents drawn by the converter and consequently the system currents are distorted as well, Fig. 6.14. The output voltages and system currents' THD during the fault, are presented in Fig. 6.15.

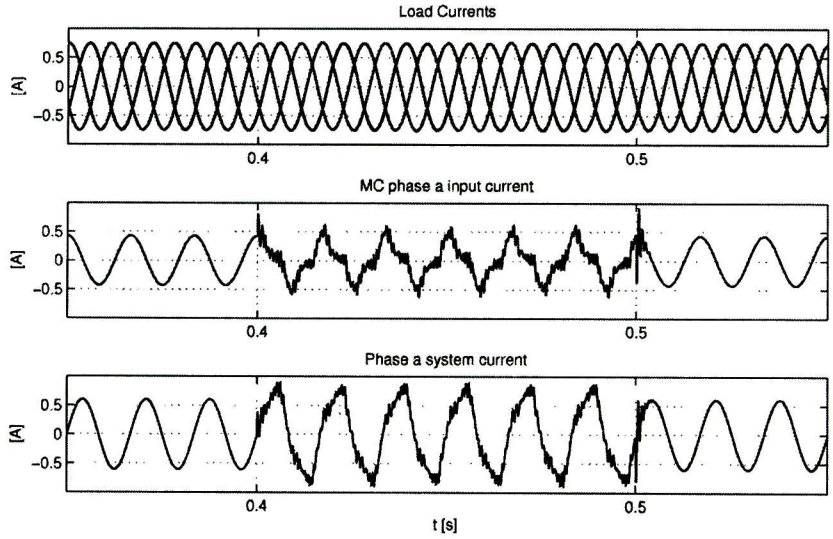


Figure 6.14. DVR response under unbalanced voltage variation. From top to bottom: Load currents, matrix converter phase *a* input current and supply system current phase *a*.

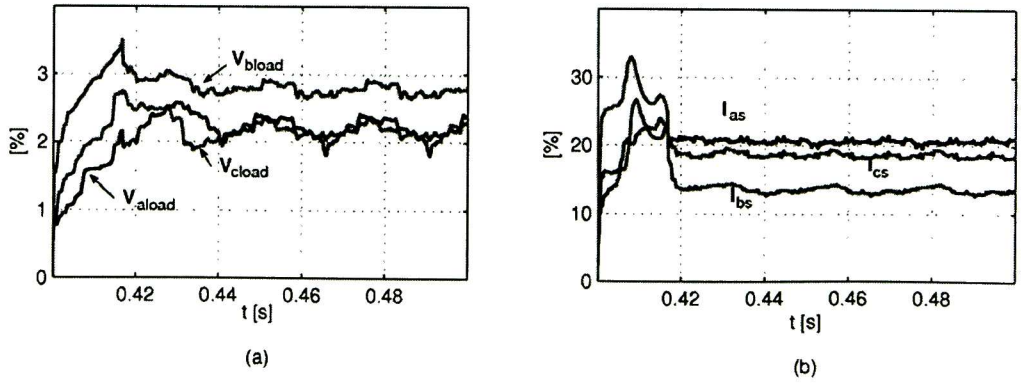


Figure 6.15. a) Load voltages' THD. b) System supply currents' THD.

Once evidenced the capability of the proposed DVR topology 1 to operate satisfactorily before unbalanced conditions, its behavior under distorted input voltages will be evaluated..

In such case, a 5th harmonic is added into phases *a* and *c*, an a 7th harmonic component into phase *b*. The magnitudes of the harmonics added are 0.2 times the fundamental component in each phase. Output filter values used in this study case were: R_{of} = 70Ω, L_{of} = 5 mH and Cof = 5 μF. Voltage compensator response is illustrated in Figs. 6.16-6.18.

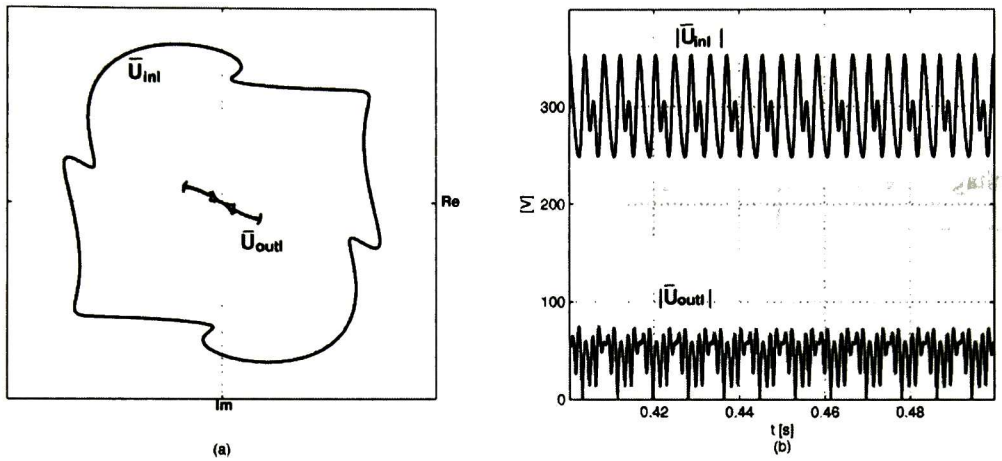


Figure 6.16. a). $\overline{U}_{inl}$ and $\overline{U}_{outl}$ in the complex space. b) Vectors magnitude

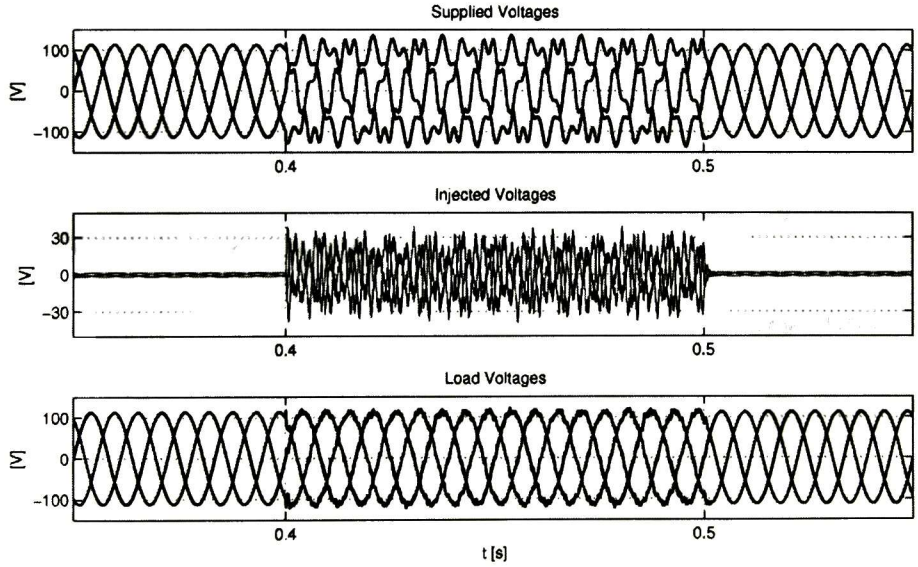


Figure 6.17. DVR response under voltage with harmonic distortion. From top to bottom: Supply system voltages, injected voltages and load voltages.

Again, the matrix converter does not have difficulties to synthesize the required voltages for compensation, Fig. 6.16. In the input voltages the low order harmonics are appreciated, but they no longer appear on the output voltages, Fig. 6.17. The THD=20% on every phase input voltage is reduced to approximately 5% on the output voltages. The harmonic content in the output signals is due to the saturation in the output filter's inductor model and the low modulation indexes.

In Fig. 6.18 it is noteworthy that the output currents' harmonic content has been filtered naturally by the RL load. By comparing input and output voltages' harmonic spectrum and THD, Fig. 6.19, it is verified that even with considerable distorted conditions in the supply voltages, the compensator operation is remarkable.

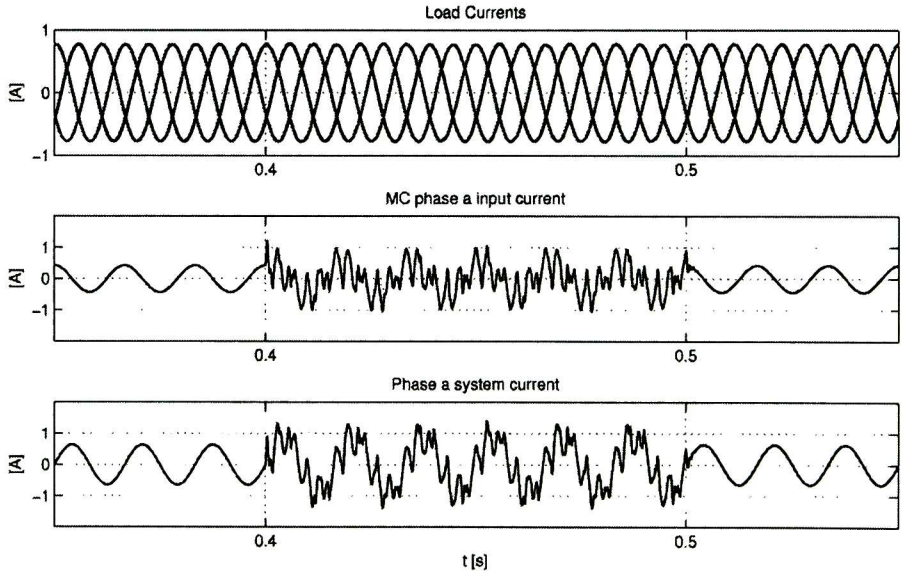


Figure 6.18. DVR response under voltage with harmonic distortion. From top to bottom: Load currents, matrix converter phase *a* input current and supply system phase *a* current.

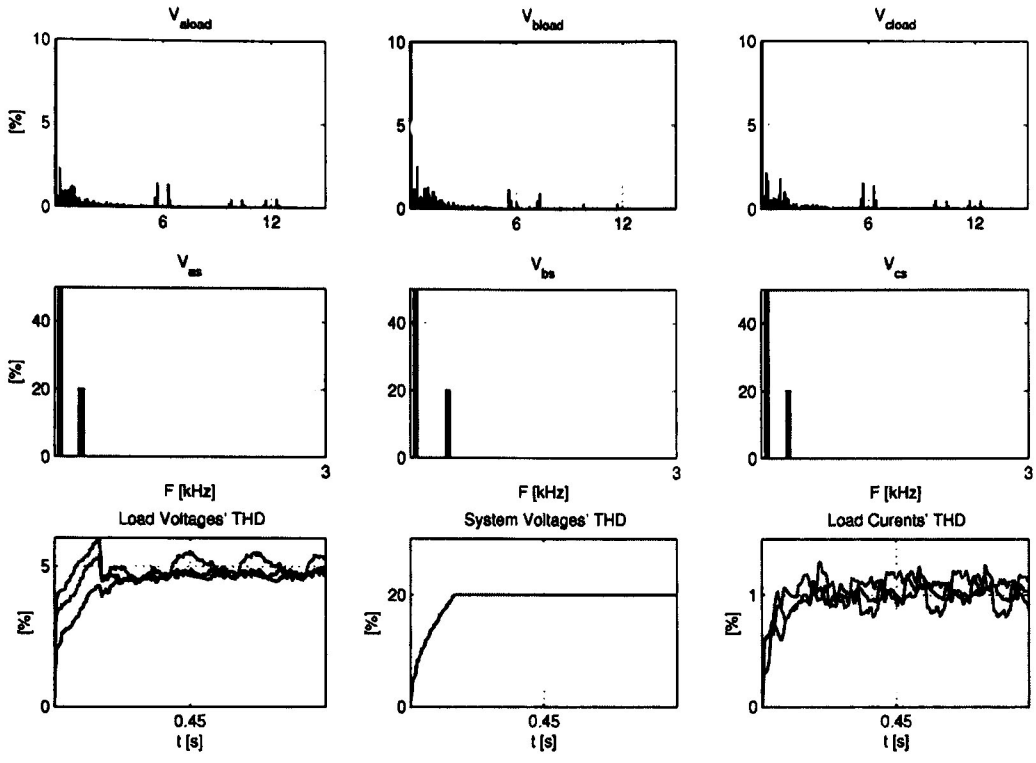


Figure 6.19. From top to bottom: Harmonic content of load voltages, harmonic content of system voltages and main signals' THD.

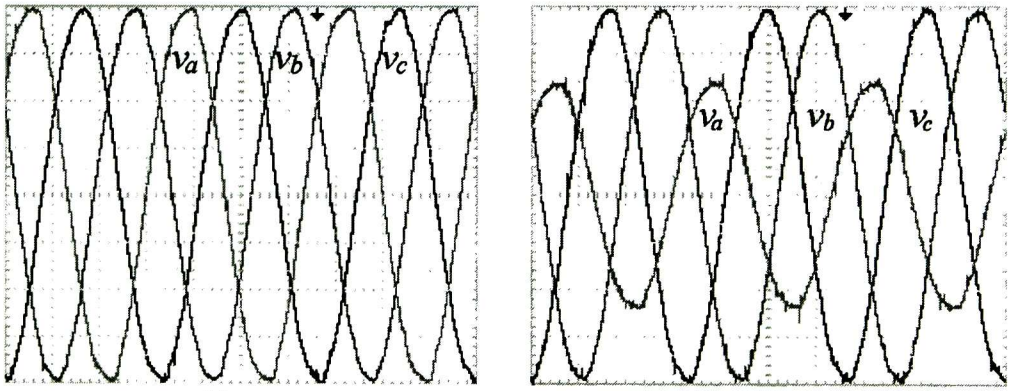
6.2.2 Experimental results

The major parameters utilized for experimental tests are listed in Table 6.2. Some parameters' values are different from the ideal ones shown in Table 6.1, and this is due to unavailability of all components at that time in the laboratory.

Table 6.2. System Parameters

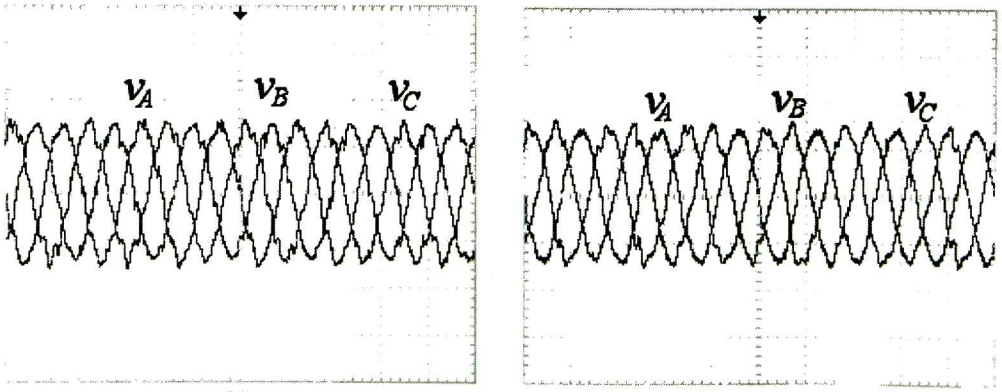
Parameter	Value
C_{if}: Input filter capacitor	10 μF
L_{if}: Input filter inductor	2.1 mH
C_{of}: Output filter capacitor	4.7 μF
L_{of}: Output filter inductor	2.2 mH
R_{of}: Output filter resistor	171 Ω
L_{load}: Load Inductor	213 mH
R_{load}: Load Resistor	120 Ω

The voltage sag correction and the harmonic suppression performance of the system are verified by means of several experimental tests. The voltages and currents comparison presented in Figs 6.20, 6.21 and 6.22 exhibits the performance of the compensator for an unbalanced case, where a 37.5% voltage sag was applied on phase *a*. The load voltages magnitudes remain almost undisturbed during the time of analysis which means the control strategy is able to reject the disturbance. The evident distortion in the load voltages during both conditions is partly due to the saturation of the inductors used in both filters (input/output), because low frequency inductors were used. A second aspect to be considered in order to explain the distortion is the modulation index. Before the sag takes place, a very low modulation index was used; that is why the distortion is more noticeable during pre-sag condition. Anyway, as in the simulated waveforms exposed, the load voltages are fully maintained, which demonstrate the effectiveness of the DVR. Likewise, during the fault the load currents remain almost invariant.



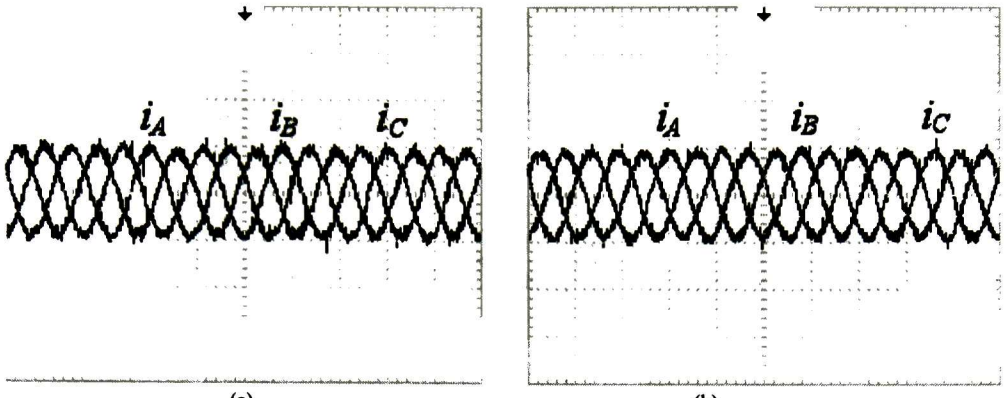
(a) (b)

Figure 6.20. Supply voltages during the unbalanced voltage sag test. a) Pre-sag condition. b) Sag condition. (20V/div,5ms/div)



(a) (b)

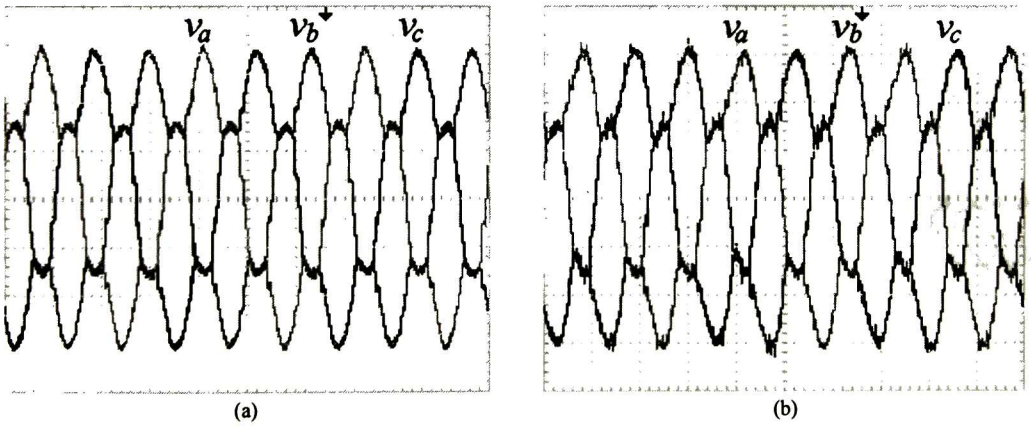
Figure 6.21. Load voltages during the unbalanced voltage sag test. a) Pre-sag condition. b) Sag condition. (50V/div, 10ms/div)



(a) (b)

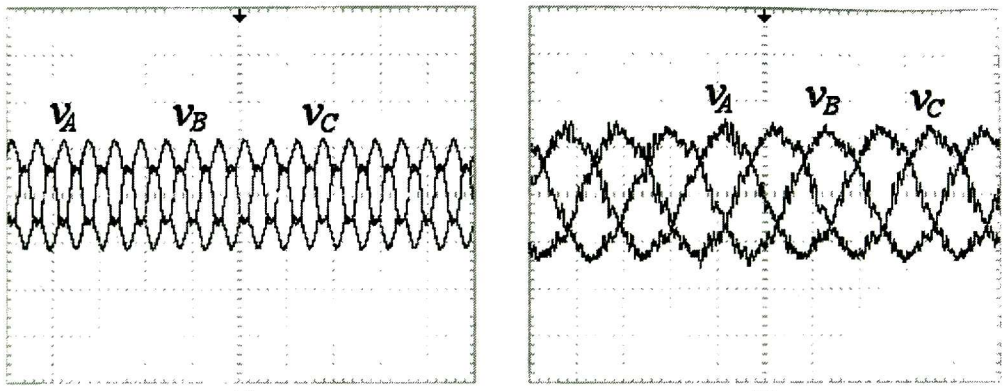
Figure 6.22. Load currents during the unbalanced voltage sag test. a) Pre-sag condition. b) Sag condition. (0.5A/div,10ms/div)

The latter study case involves harmonic distortion in the supply voltages, provoked by a nonlinear load supplied by the same feeder. The nonlinear load was a diode bridge rectifier with a resistive load. As it can be seen on Fig. 6.25, the 5^{th} and 7^{th} harmonic components are reduced by a factor of 20 and 15 dB respectively, after compensating action was performed. In this way the total harmonic distortion (THD) is also reduced since these harmonics are the most dominant in the system voltage spectrum. In Figs. 623, 6.24 and 6.26 voltages and currents with and without compensation are displayed. For the no-compensation condition the matrix converter was operated with a zero reference voltage. Note that in the load voltage after compensation was performed, some high order harmonic components still exist which can be generated by the saturation characteristics of the inductor in the output filter. Nevertheless, the effects of these harmonics are minimal for the load as it is shown in Fig. 6.26.



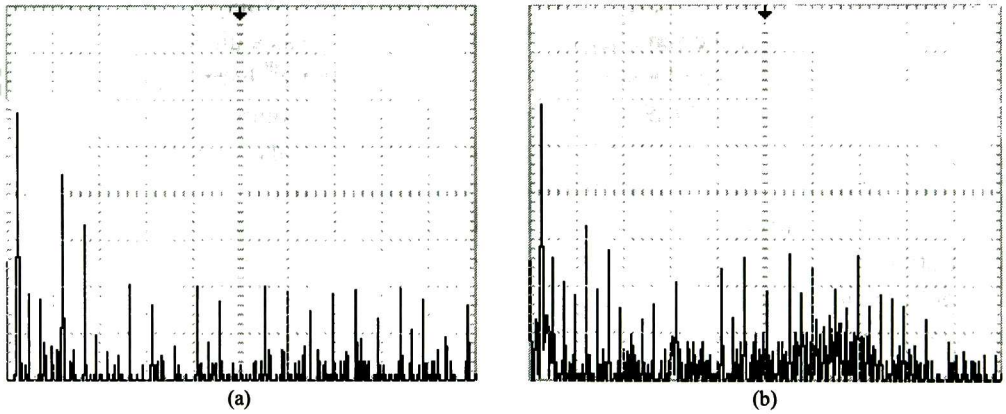
(a) (b)

Figure 6.23. Supply voltages during the distorted voltage test. a) No-compensation condition. b) Compensation condition. (20V/div, 5ms/div)



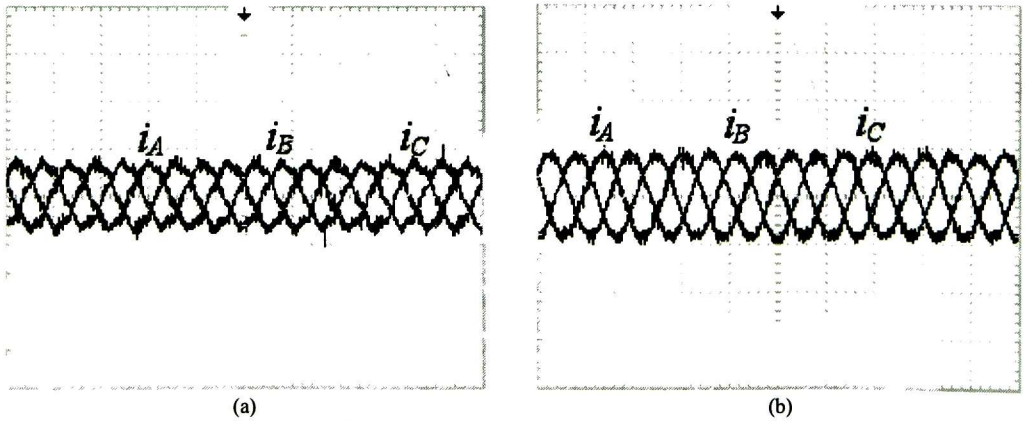
(a) (b)

Figure 6.24. Load voltages during the distorted voltage test. a) No-compensation condition (50V/div, 10ms/div). b) Compensation condition (50V/div, 5ms/div).



(a) (b)

Figure 6.25. Load voltages FFT during the distorted voltage test. a) No-compensation condition. b) Compensation condition. (10dB/div, 250Hz/div)



(a) (b)

Figure 6.26. Load currents during the distorted voltage test. a) No-compensation condition. b) Compensation condition. (0.5A/div, 10ms/div)

6.3 DVR Topology 2 Results

Likewise, as with the topology 1 the performance of the whole DVR system is verified by detailed numerical simulation using PSCAD software and some experimental tests. The system key parameters for simulation are given in Table 6.2. The input filter selected for this topology is a RLC filter as the one illustrated in Fig. 6.5, with a cut-off frequency of 318 Hz and a 20Ω damping resistor. The matrix converter-based DVR with the proposed topology 2, Fig. 6.27, is utilized for balanced and unbalanced voltage sags and swells compensation.

Table 6.2 System 2 Parameters

Parameter	Value
C_{if}: Input Filter Capacitor	50 μF
R_{if}: Input Filter Resistance	1 Ω
C_{of}: Output Filter Capacitor	6 μF
L_{of}: Output Filter Inductor	1.2 mH
L_{load}: Load Inductor	33.6 mH
R_{load}	20 Ω

6.3.1 Numerical verification

For the case of balanced sag, a 50% three-phase voltage sag in the supply voltage is simulated, lasting for 0.08s. Voltage and current waveforms during the voltage sag period are plotted in the *abc* reference frame, Figs. 6.28 and 6.29. It can be observed that the DVR is able to maintain the voltage load almost undisturbed during the sag period, by injecting the appropriate compensation. Load voltages' THD are about 4% during the disturbance, as Fig. 6.30 illustrates.

The fast response of the control is illustrated through the load current plot. The currents flowing from the supply into the matrix converter increase during the sag, but both currents shows not considerable harmonic distortion as expected. The system currents' distortion also depends in the currents magnitude demanded by the load.

In the second test, the DVR performance is evaluated under an unbalanced voltage variation. For this test, voltage sags of 20% and 40% in phase *b* and *c*, respectively, are considered. Furthermore, a 17% voltage swell is applied on phase *a*. The DVR response for unbalanced test is illustrated in Figs. 6.31 and 6.32.

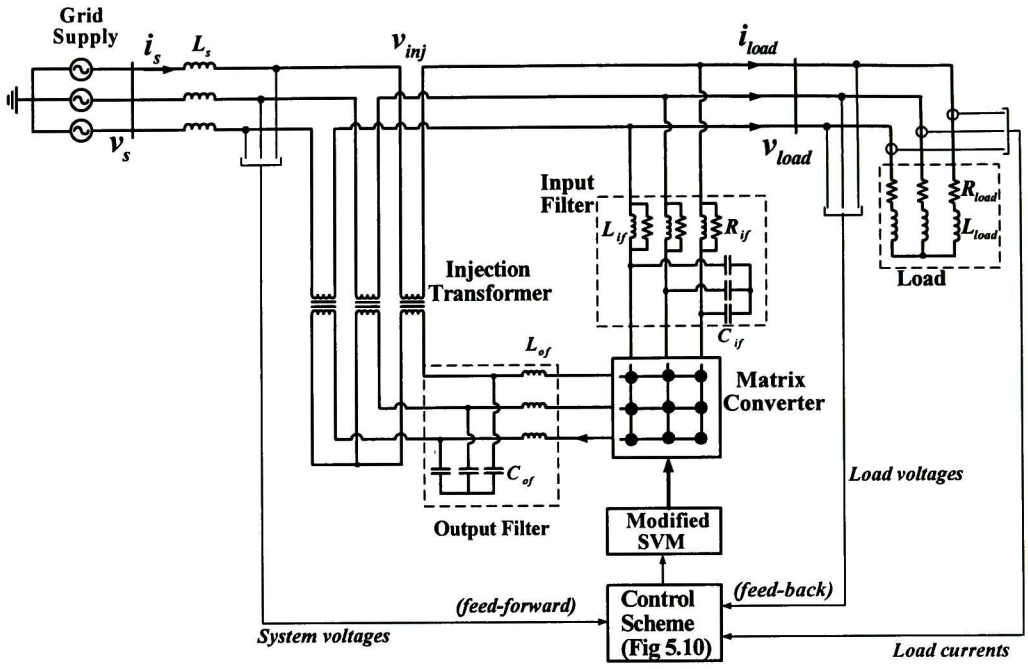


Figure 6.27. Proposed DVR topology 2 system architecture

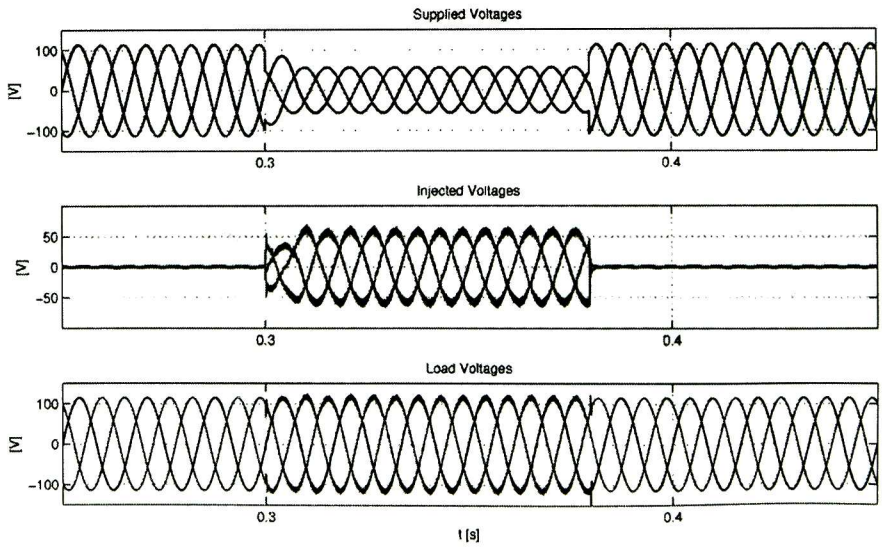


Figure 6.28. DVR response for balanced voltage sag compensation. From top to bottom: Supply voltages, Injected voltages and Load voltages.

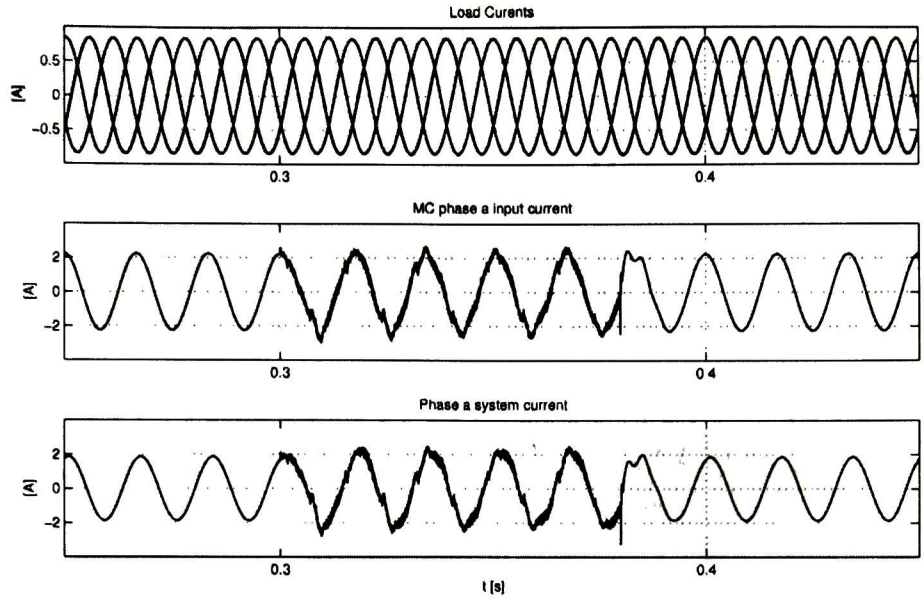


Figure 6.29. DVR response for balanced voltage sag compensation. From top to bottom: Load currents, Matrix converter phase a input current and Phase *a* supply system current.

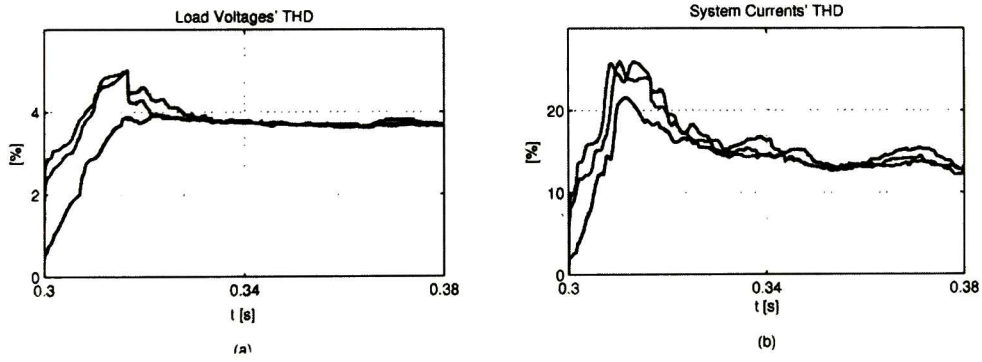


Figure 6.30. a) Load voltages' THD. b) System currents' THD

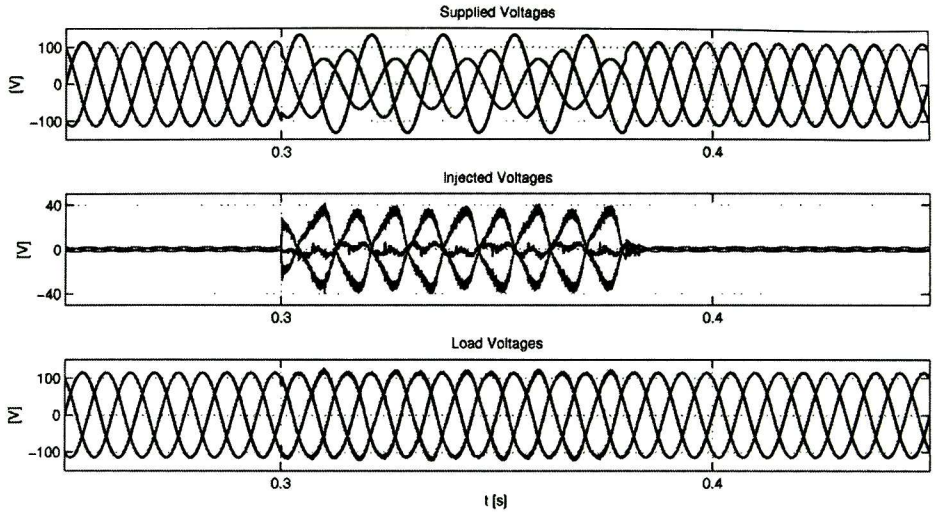


Figure 6.31. DVR response for unbalanced voltage disturbance. From top to bottom: Supply voltages, Injected voltages and Load voltages

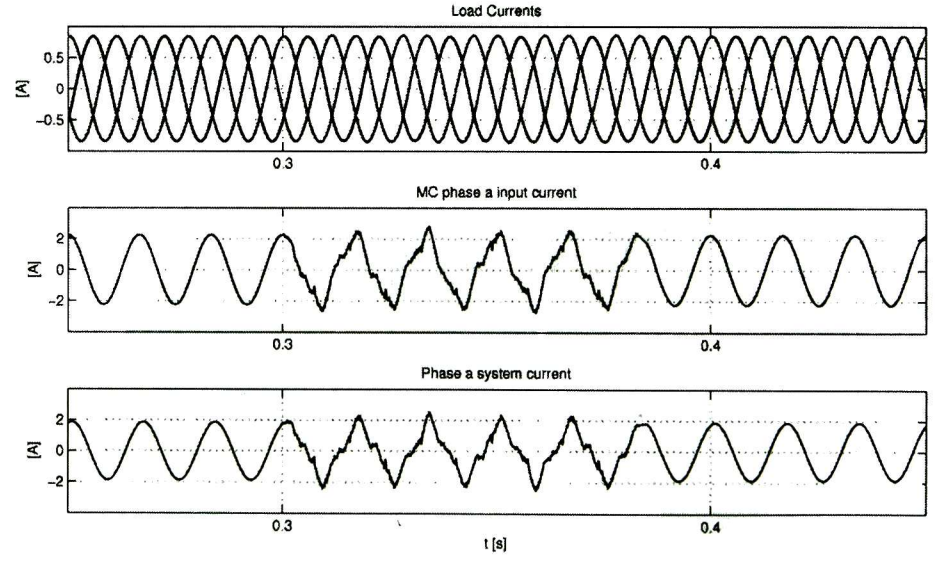


Figure 6.32. DVR response for unbalanced voltage disturbance. From top to bottom: Load currents, Matrix converter phase *a* input current and Phase *a* supply system current.

The DVR is able to reduce the percent of imbalance from 22.17%, to 1.1% approximately, which demonstrate the effectiveness of this proposition. The supplied system currents show a higher harmonic content, Fig. 6.33, compared to the previous study case because of the harmonics generated in the currents drawn by the matrix converter. However, this condition does not affect the overall performance. The load voltages maintained and average THD less than 5%.

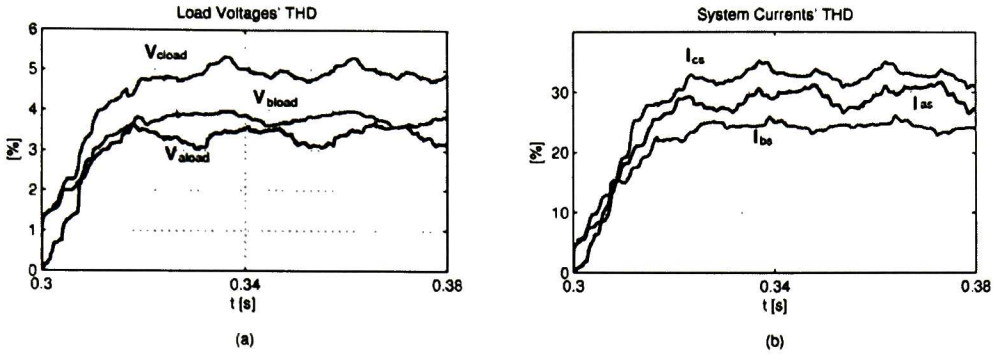


Figure 6.33. a) Load Voltages' THD. b) System currents' THD

6.3.2 Experimental results

As was established in chapter 5, present DVR topology is more suited to compensate deep-level voltage sags than topology 1. An experimental test was carried out to verify the previous statement; hence, a symmetric voltage sag of 46 % is applied at the system supply voltages. In Fig. 6.34, a comparison between supply and load voltages, in one phase, is illustrated for pre-sag and sag conditions.

Results are similar to the simulation's results in which despite of the disturbance the load current amplitudes do not suffer evident variations, Fig. 6.35.

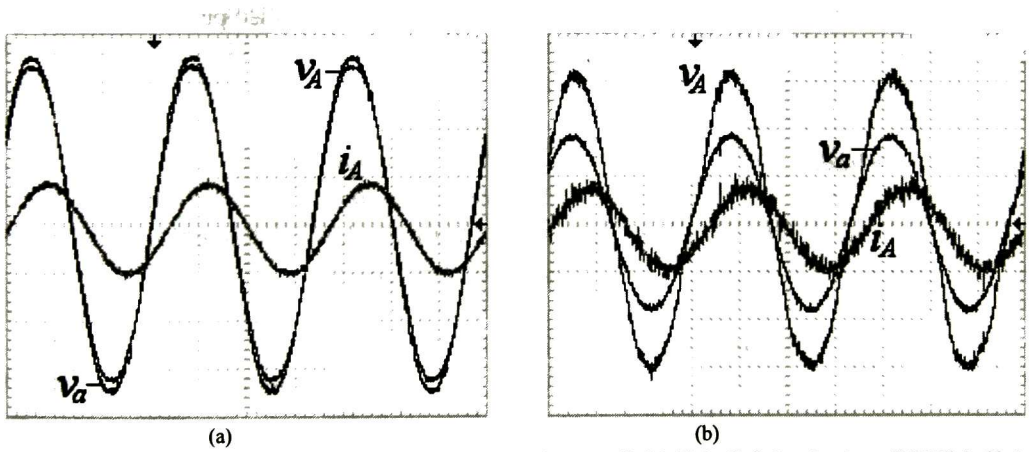
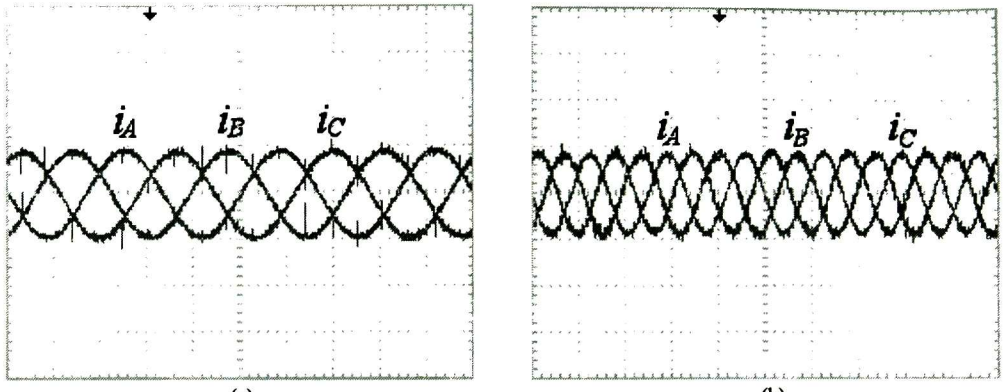


Figure 6.34. a) Pre-sag condition. b) Sag condition. Ch 1: Load current (0.5 A/div), Ch 2: Load voltage (20V/div), Ch 3: Supply voltage (20V/div, 5ms/div).



(a) (b)

Figure 6.35. a) Pre-sag condition (0.5 A/div, 5ms/div). b)Sag condition. Load currents (0.5 A/div, 10ms/div).

6.4 Conclusions

To demonstrate the validity of the proposed topologies, the matrix converter based-DVR has been implemented. The experiments have been performed under low voltage conditions. To precisely control the output voltage, the proposed MDSVM along with the software routines of the controller were programmed in the board eZdsp-TMS320F2812. Details on the prototype design and the complete control scheme were also explained.

In order to validate the proposed topologies several cases were analyzed. The results obtained showed that the proposed scheme controls the output voltage fast and accurately for the different disturbances conditions. Experimental results were also provided, verifying this approach.

6.5 References

[6.1] Luis Carlos Herrero de Lucas, "Estudio y simulación de convertidores CA/CA directos 3Φx3Φ en matriz de conversión controlados mediante sliding en fuente de corriente," *Tesis de doctorado, Departamento de Tecnología Electrónica, Universidad de Valladolid*, Valladolid, Feb. 2005.

[6.2] Jiabin Wang and M. Bouazdia: "Influence of filter parameters/topologies on stability of matrix converter-fed permanent magnet brushless motor drive systems," *IEEE International Electrical Machines and Drives Conference, IEMDC'09*, pp. 964-970, 2009.

[6.3] D. D. Solin, T. E. Grebe, M. F. Granaghan, and A. Sundarm: "Statistical analysis of voltage DIP's and interruption-Final results from the EPRI distribution system power quality monitoring survey", in *Proc. CIRED'99*, ch. 2, 1999.

CHAPTER VII

Conclusions and Future Work

7.1 Conclusions

This dissertation proposed two novel DVR topologies based on the AC-AC matrix converter to cope with power quality issues presented in distribution systems. The developing of the proposed Modified Direct Space Vector Modulation (MDSVM) allows the incorporation of matrix converter technology into the conventional DVR configuration which results in a cost-effective and multifunctional solution. Likewise, the use of AC-AC energy conversion technology instead of the traditional DC-AC allows eliminating all the drawbacks associated to the DC-link and increases the device's reliability.

A literature survey regarding power quality issues and a discussion of the modern solution commonly employed in industrial applications were presented. Based on the analyzed information the objectives of the present research were established.

According to the specialized literature the traditional DVR is the best option in applications concerning voltage compensation. However, AC-AC energy conversion technology has emerged as a novel solution. Advantages such as bidirectional power flow, high power density, high quality input currents and the lack of energy storage devices, etc., ratifies the actual trend.

On the other hand, among the different AC-AC converters, the matrix converter has been selected as the device with better features. However, despite all the advantages offered by this converter, some disadvantages have delayed its industrial implementation. In order to accelerate the maturation process of this technology and to expand its application field, the MDSVM was developed. The proposed strategy is based on the control of the reference vectors in the complex, allowing the matrix converter to generate totally controllable

voltages, characteristic that leads to the novel DVR topologies proposed. The main features of the MDSVM:

- Generation of balanced output voltages despite the condition of the input voltages
- Generation of input currents with an acceptable harmonic content.
- Amplitude and frequency control in the output voltages
- Input power factor controllable
- Fast and accurate generation of the reference voltages in spite of its condition.

In order to verify the performance of the matrix converter with the MDSVM, several simulations were carried out considering different conditions. The results obtained indicate that the matrix converter is able to synthesize a great variety of reference voltages departing from distorted supply voltages, as long as the operative restrictions of the converter are fulfilled. Taking into account these characteristics, a voltage compensator based on the matrix converter was designed.

The voltage regulation is performed through a controller build by the combination of feed-back and feed-forward control branches. The feed-back control loop is used to achieve zero steady state error, while the feed-forward branch has been included to accelerate the dynamic response and reduce the overvoltage at restoration.

Finally, to validate the functionality of the DVR topologies proposed, a laboratory-scale prototype was implemented. Several experimental tests elucidate the capabilities of the proposed topologies. Topology 1 is able to compensate symmetric voltage drops up to 43 %. Besides it is able to compensate voltage imbalanced and mitigate the presence of voltage harmonics. Topology 2, is suitable for deep-level voltage sags, theoretically it can compensate sags up to 80%, but experimentally it has been proven that after sags of 60% the system becomes unstable.

In conclusion, the DVR topologies operates satisfactorily before each analyzed condition, that is why it is proposed as an cost-effective solution to mitigate the power quality problems presented in power distribution systems.

7.2 Contributions

The main contributions of current research work are summarized as follows:

- The Mathematical development of the MDSVM strategy to control the matrix converter operation. The proposed technique allows the converter to generate an

totally controllable output voltage despite the adverse existing conditions in the input voltages.

- The design of two novel multi-functional DVR topologies, proposed to improve the power quality in distribution systems. The matrix converter based DVR is aimed to compensate asymmetric and asymmetric voltage disturbances as well as filter voltage harmonics components and power factor correction.

- Development of a detailed model of the DVR topologies in order to evaluate their dynamic behavior through simulations in time-domain performed in PSCAD software.

- Development of mathematical models of the DVR topologies intended for future stability and power flow control analysis.

- Design and implementation of a laboratory-scale prototype of the matrix converter-based DVR.

- Implementation of the MDSVM strategy, voltage controller software routines and four-step commutation strategy in the DSP based board eZdsp-TMS320F2812.

7.3 Recommendations for future work

Regarding the research developed so far, the following topics are proposed as possible future research:

- Confirm the validity of the proposed topologies under higher power ratings

- Analyze the stability of the electric systems when the matrix converter based DVR is incorporated.

- Investigate the performance of the matrix converter in power flow control applications.

- Design and implementation of a robust and adaptive control algorithm, it can be based in neural networks or fuzzy logic.

- Analyze the performance of the proposed DVR topologies when feeding non-linear loads.

7.4 Activities developed during the Ph. D.

- Doctoral Fellowship: At the Institute of Energy Technology, Aalborg University, Denmark, From January 2008 to October 2008.
- Conference: Modern Electric Power Systems International Symposium, MEPS'2010, held in Wroclaw, Poland.

7.5 List of Publications

- Juan M. Ramírez, José M. Lozano y Julio Rosas C., "Sags, Swells and Harmonic Solid State Compensator", *Proceedings on IEEE Industrial Electronics Conference 2006, IECON'06*, Paris, France, Nov. 2006.

- Juan M. Ramírez and José M. Lozano, "Matrix converter performance under unbalanced input voltages", *40th North American Power Symposium, NAPS'08* Calgary, Canada, Sep. 2008.

- José M. Lozano, Juan M. Ramírez, "AC-AC converter for unbalanced supply," *19th International Symposium on Power Electronics, Electrical Drives, Automation and Motion, SPEEDAM '08*, Ischia, Italy. July 2008.

- José M. Lozano, Juan M. Ramírez and Rosa Elvira C. "A novel dynamic voltage restorer based on matrix converters," *Modern Electric Power Systems International Symposium, MEPS'2010*, Wroclaw, Poland Sep. 2010.

- Juan M. Ramírez, José M. Lozano, "Voltage compensator based on ac-ac converters," submitted for publication to *Electric Power Research*, Ms. Ref. No. EPSR-D07-00819R1.

- Antonio Valderrabano, Juan M. Ramírez and José M. Lozano, "Implementation of a 84-pulse voltage source converter for special applications," submitted for publication to *Electric Power Components and Systems*, Manuscript ID. UEMP-2010-0705.

APPENDIX A

Commutation Vectors

In this appendix all the possible states for the matrix converter switches represented in the Park's complex space are exhibited, for a set of three phase balanced voltages.

A.1 Input-voltage vectors in the complex space

Park's vector is applied to systems with three magnitudes and two degrees of freedom. Considering a system with a set of three-phase balanced voltages defined as,

$$\begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} = \begin{bmatrix} V_{in}\sin(\omega t) \\ V_{in}\sin\left(\omega t - \frac{2\pi}{3}\right) \\ V_{in}\sin\left(\omega t + \frac{2\pi}{3}\right) \end{bmatrix} \tag{A.1}$$

The line-to-line input-voltages will be,

$$\begin{bmatrix} v_{ab}(t) \\ v_{bc}(t) \\ v_{ca}(t) \end{bmatrix} = \begin{bmatrix} \sqrt{3}V_{in}\sin\left(\omega t + \frac{\pi}{6}\right) \\ \sqrt{3}V_{in}\sin\left(\omega t - \frac{\pi}{2}\right) \\ \sqrt{3}V_{in}\sin\left(\omega t + \frac{5\pi}{6}\right) \end{bmatrix} \tag{A.2}$$

The Park's vectors of the input-voltages are defined by:

$$\overline{U}_{imp}(t)=\frac{2}{3}\left(v_a(t)+v_b(t)e^{j\frac{2\pi}{3}}+v_c(t)e^{j\frac{4}{3}}\right) \tag{A.3}$$

$$\overline{U}_{inl}(t)=\frac{2}{3}\left(v_{ab}(t)+v_{bc}(t)e^{j\frac{2\pi}{3}}+v_{ca}(t)e^{j\frac{4}{3}}\right) \tag{A.4}$$

which both vectors rotate at a speed of ωt.

A.2 Switching States

The matrix converter consists of nine bidirectional switches arranged in three groups, each being associated with an output line. This bi-directional switches arrangement connects any of the input lines to any of the output lines, Fig A.1. A matrix with elements *Hij*, representing the state of each bidirectional switch (*on=1, off=0*) leads to a 2^9 possible combinations. Nonetheless, for ensure a matrix converter proper operation just one and only one power switch in each column must be active at any instant. This restriction reduces the permitted configuration of the conversion matrix from 512 to 27 switching states, as indicated in Table A.1.

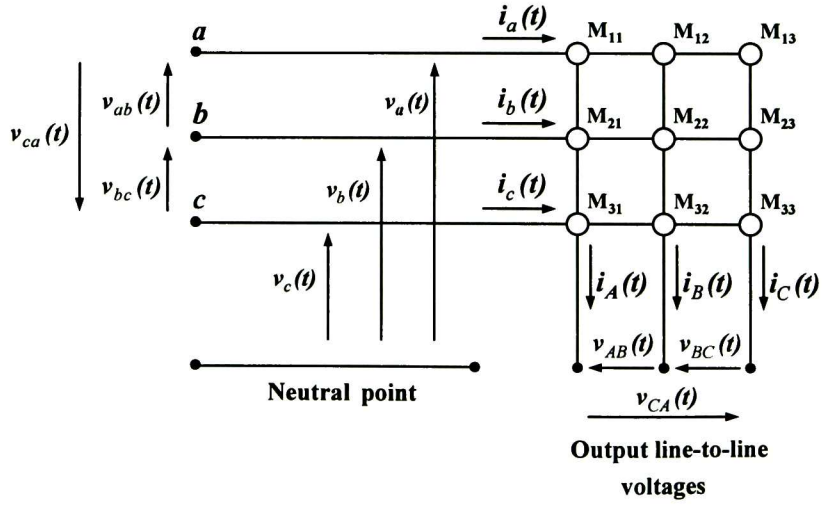


Figure A.1. Conversion matrix basic structure

A.2.1 Switching states analysis

For any switching state the output-voltage and the input-current complex vectors are defined as:

$$\bar{U}_{outl}(t) = \left(v_{AB}(t) + v_{BC}(t) e^{j\frac{2\pi}{3}} + v_{CA}(t) e^{j\frac{4}{3}} \right) \tag{A.5}$$

$$\bar{I}_{in}(t) = \left(i_a(t) + i_b(t) e^{j\frac{2\pi}{3}} + i_c(t) e^{j\frac{4}{3}} \right) \tag{A.6}$$

where the modulus and argument depend on the active state. Because of that, is necessary to carry out an individual analysis for each state represented in Table A.1. As an example the state S2, Fig A.2, is analyzed as follows. The input/output voltages relationships can be stated by:

$$\begin{aligned} v_{AB}(t) &= 0 \\ v_{BC}(t) &= v_{ab}(t) \\ v_{CA}(t) &= -v_{ab}(t) \end{aligned} \tag{A.7}$$

The Park's vector of the output-voltage is,

$$\left|\bar{U}_{out}(t)\right| = \sqrt{3} \cdot v_{1ab}(t) \qquad \angle \bar{U}_{out}(t) = \frac{\pi}{2} \tag{A.8}$$

Eq. (A.8) defines a fixed position vector with a time-varying modulus. The input/output currents relationships are,

$$\begin{aligned} i_a(t) &= i_A(t) + i_B(t) = -i_C(t) \\ i_b(t) &= i_C(t) \\ i_c(t) &= 0 \end{aligned} \tag{A.9}$$

The corresponding Park's vector is,

$$\left|\bar{I}_{in}(t)\right| = \sqrt{3} \cdot i_C(t) \qquad \angle \bar{I}_{in}(t) = \frac{5\pi}{6} \tag{A.10}$$

representing a fixed vector too.

Table A.1 Permitted switching states in a three phase to three phase matrix converter

STATE	H_{11}	H_{12}	H_{13}	H_{21}	H_{22}	H_{23}	H_{31}	H_{32}	H_{33}
S1	1	1	1	0	0	0	0	0	0
S2	1	1	0	0	0	1	0	0	0
S3	1	1	0	0	0	0	0	0	1
S4	1	0	1	0	1	0	0	0	0
S5	1	0	0	0	1	1	0	0	0
S6	1	0	0	0	1	0	0	0	1
S7	1	0	1	0	0	0	0	1	0
S8	1	0	0	0	0	1	0	1	0
S9	1	0	0	0	0	0	0	1	1
S10	0	1	1	1	0	0	0	0	0
S11	0	1	0	1	0	1	0	0	0
S12	0	1	0	1	0	0	0	0	1
S13	0	0	1	1	1	0	0	0	0
S14	0	0	0	1	1	1	0	0	0
S15	0	0	0	1	1	0	0	0	1
S16	0	0	1	1	0	0	0	1	0
S17	0	0	0	1	0	1	0	1	0
S18	0	0	0	1	0	0	0	1	1
S19	0	1	1	0	0	0	1	0	0
S20	0	1	0	0	0	1	1	0	0
S21	0	1	0	0	0	0	1	0	1
S22	0	0	1	0	1	0	1	0	0
S23	0	0	0	0	1	1	1	0	0
S24	0	0	0	0	1	0	1	0	1
S25	0	0	1	0	0	0	1	1	0
S26	0	0	0	0	0	1	1	1	0
S27	0	0	0	0	0	0	1	1	1

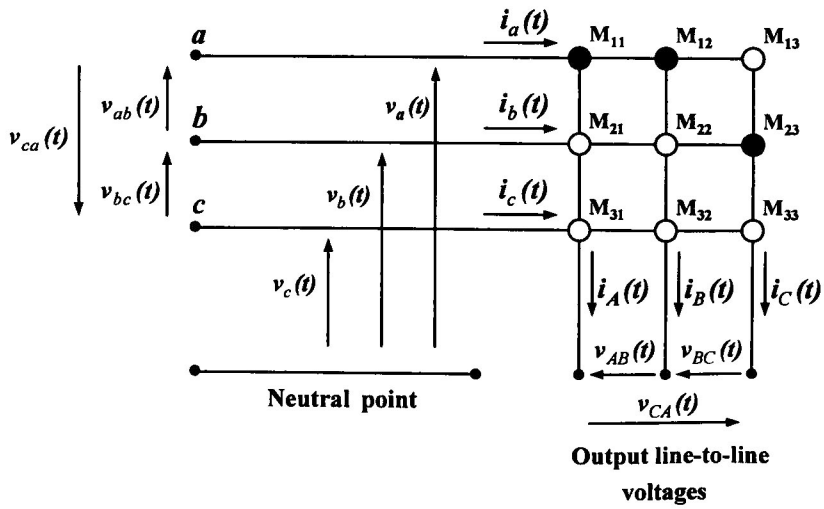


Figure A.2. Conversion matrix topology for state S2.

Following a similar procedure it is possible to determine the output-voltage and input current complex vectors for all the permitted switching states. From the states analysis it can be concluded that among the 27 switching configurations:

- Six switching states provide a direct connection of each output line to a different input line, producing a rotating voltage vector with amplitude and frequency similar to the input voltage system and direction dependant on the sequence: synchronous or inverse.
- Eighteen switching states produce active vectors, of variable amplitude, depending on the selected line-to-line voltage, but of stationary position.
- The last three switching states produce a zero vector, by connecting all the output lines to the same input line.

Tables A.2-A.4 summarize the results obtained. Figs A.3-A.4 depict a set of vectors at time t = 0.

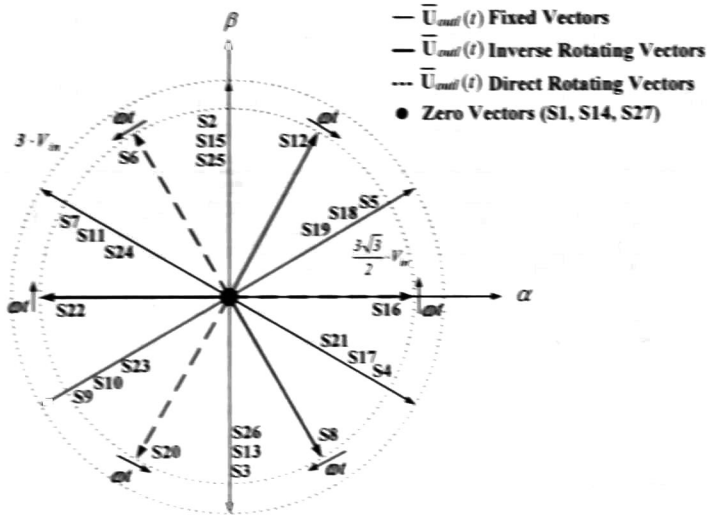


Figure A.3 Vectors $\overline{U}_{out}(t)$ in the complex space

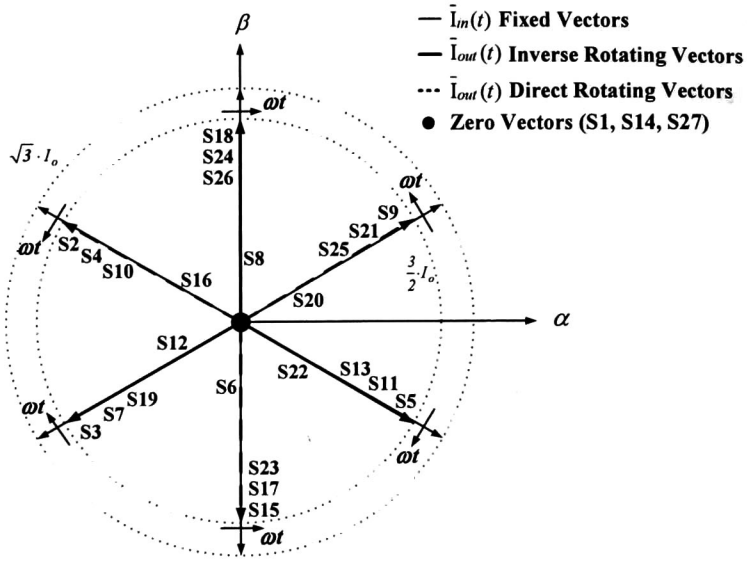


Figure A.4 Vectors $\bar{I}_{in}(t)$ and $\bar{I}_{out}(t)$ in the complex space

Table A.2. Parks' vector arguments and modulus of line-to-line output voltage and input current for each commutation state (Zero Vectors)

ZERO VECTORS				
STATE	$\lvert\bar{U}_{out}\rvert$	$\angle\bar{U}_{out}$	$\lvert\bar{I}_{in}\rvert$	$\angle\bar{I}_{in}$
S1 (aaa)	**0**	**0**	**0**	**0**
S14 (bbb)	**0**	**0**	**0**	**0**
S27 (ccc)	**0**	**0**	**0**	**0**

Table A.3. Parks' vector arguments and modulus of line-to-line output voltage and input current for each commutation state (Rotating Vectors)

ROTATING VECTORS				
STATE	$\lvert\bar{U}_{out}\rvert$	$\angle\bar{U}_{out}$	$\lvert\bar{I}_{out}\rvert$	$\angle\bar{I}_{out}$
S6 (abc)	$3\sqrt{3}/2\cdot V_{in}$	$\omega t-\pi/3$	$3/2\cdot I_o$	$\omega t-\pi/2$
S16 (bca)	$3\sqrt{3}/2\cdot V_{in}$	$\omega t-\pi$	$3/2\cdot I_o$	$\omega t-7\pi/6$
S20 (cab)	$3\sqrt{3}/2\cdot V_{in}$	$\omega t+\pi/3$	$3/2\cdot I_o$	$\omega t-11\pi/6$
S8 (acb)	$3\sqrt{3}/2\cdot V_{in}$	$2\pi/3-\omega t$	$3/2\cdot I_o$	$\pi/2-\omega t$
S12 (bac)	$3\sqrt{3}/2\cdot V_{in}$	$-2\pi/3-\omega t$	$3/2\cdot I_o$	$7\pi/6-\omega t$
S22 (cba)	$3\sqrt{3}/2\cdot V_{in}$	$-\omega t$	$3/2\cdot I_o$	$11\pi/6-\omega t$

Table A.4. Parks' vector arguments and modulus of line-to-line output voltage and input current for each commutation state (Fixed Vectors)

FIXED VECTORS				
STATE	$\lvert\overline{U}_{out}\rvert$	$\angle\overline{U}_{out}$	$\lvert\overline{I}_{in}\rvert$	$\angle\overline{I}_{in}$
S2 (aab)	$\sqrt{3}\cdot v_{ab}(t)$	$\pi/2$	$\sqrt{3}\cdot i_C(t)$	$5\pi/6$
S3 (aac)	$\sqrt{3}\cdot v_{ca}(t)$	$-\pi/2$	$\sqrt{3}\cdot i_C(t)$	$-5\pi/6$
S4 (aba)	$\sqrt{3}\cdot v_{ab}(t)$	$-\pi/6$	$\sqrt{3}\cdot i_B(t)$	$5\pi/6$
S5 (abb)	$\sqrt{3}\cdot v_{ab}(t)$	$\pi/6$	$\sqrt{3}\cdot i_A(t)$	$-\pi/6$
S7 (aca)	$\sqrt{3}\cdot v_{ca}(t)$	$5\pi/6$	$\sqrt{3}\cdot i_B(t)$	$-5\pi/6$
S9 (acc)	$\sqrt{3}\cdot v_{ca}(t)$	$-5\pi/6$	$\sqrt{3}\cdot i_A(t)$	$\pi/6$
S10 (baa)	$\sqrt{3}\cdot v_{ab}(t)$	$-5\pi/6$	$\sqrt{3}\cdot i_A(t)$	$5\pi/6$
S11 (bab)	$\sqrt{3}\cdot v_{ab}(t)$	$5\pi/6$	$\sqrt{3}\cdot i_B(t)$	$-\pi/6$
S13 (bba)	$\sqrt{3}\cdot v_{ab}(t)$	$-\pi/2$	$\sqrt{3}\cdot i_C(t)$	$-\pi/6$
S15 (bbc)	$\sqrt{3}\cdot v_{bc}(t)$	$\pi/2$	$\sqrt{3}\cdot i_C(t)$	$-\pi/2$
S17 (bcb)	$\sqrt{3}\cdot v_{bc}(t)$	$-\pi/6$	$\sqrt{3}\cdot i_B(t)$	$-\pi/2$
S18 (bcc)	$\sqrt{3}\cdot v_{bc}(t)$	$\pi/6$	$\sqrt{3}\cdot i_A(t)$	$\pi/2$
S19 (caa)	$\sqrt{3}\cdot v_{ca}(t)$	$\pi/6$	$\sqrt{3}\cdot i_A(t)$	$-5\pi/6$
S21 (cac)	$\sqrt{3}\cdot v_{ca}(t)$	$-\pi/6$	$\sqrt{3}\cdot i_B(t)$	$\pi/6$
S23 (cbb)	$\sqrt{3}\cdot v_{bc}(t)$	$-5\pi/6$	$\sqrt{3}\cdot i_A(t)$	$-\pi/2$
S24 (cbc)	$\sqrt{3}\cdot v_{bc}(t)$	$5\pi/6$	$\sqrt{3}\cdot i_B(t)$	$\pi/2$
S25 (cca)	$\sqrt{3}\cdot v_{ca}(t)$	$\pi/2$	$\sqrt{3}\cdot i_C(t)$	$\pi/6$
S26 (ccb)	$\sqrt{3}\cdot v_{bc}(t)$	$-\pi/2$	$\sqrt{3}\cdot i_C(t)$	$\pi/2$

CENTRO DE INVESTIGACIÓN Y DE ESTUDIOS AVANZADOS DEL I.P.N.
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El Jurado designado por la Unidad Guadalajara del Centro de Investigación y de Estudios Avanzados del Instituto Politécnico Nacional aprobó la tesis

Topologías del DVR basadas en un convertidor matricial para mejorar la calidad de la energía en sistemas de distribución

DVR's Topologies matrix converter-based for improving power quality in distribution systems

del (la) C.

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