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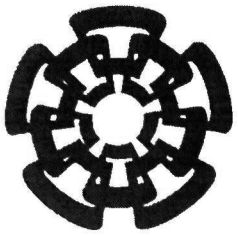


Centro de Investigación y de Estudios Avanzados
del Instituto Politécnico Nacional
Unidad Guadalajara

Diseño e Implementación de un Convertidor de 84 Pulsos

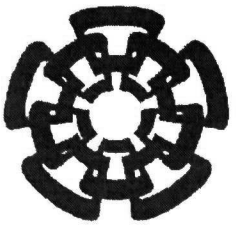
Tesis que presenta:
Antonio Valderrábano González

para obtener el grado de:
Doctor en Ciencias

en la especialidad de:
Ingeniería Eléctrica

Director de Tesis
Dr. Juan Manuel Ramírez Arredondo

CINVESTAV del IPN Unidad Guadalajara, Guadalajara, Jalisco, Diciembre de 2010.



Centro de Investigación y de Estudios Avanzados

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Unidad Guadalajara

84-Pulses Converter: Design and Assembling

A dissertation submitted by:
Antonio Valderrábano González

For the degree of:
Doctor of Sciences

In the specialty of:
Electrical Engineering

Advisor:
Dr. Juan Manuel Ramírez Arredondo

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Becario de CONACYT, expediente no. 203405

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Dedicatoria

A Anabel, por confiar en mi y darme su apoyo incondicional en estos años dedicados al doctorado

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Resumen

Este trabajo describe el uso del Compensador Estático Síncrono (StatCom) en la compensación de potencia reactiva y la mejora en la calidad de la energía. Se hace énfasis en el diseño y ensamble de una unidad convertidora de voltaje (VSC) que cumple con el estandar IEEE 519-1992 (IEEE Prácticas Recomendadas y Requerimientos para el Control de Armónicos en Sistemas Eléctricos de Potencia). El nivel de distorsión armónica total (THD) que esta unidad convertidora de voltaje produce, permite que este acondicionador de potencia sea apropiado para aplicaciones con requerimientos estrictos de calidad. Mediante el principio de reinyección, y dado el reducido número de transistores utilizado en la topología, se logra que esta propuesta sea considerada como una solución factible en la generación de ondas senoidales. El transformador de reinyección, que es uno de los elementos más importantes en esta configuración, no requiere una relación de transformación específica, pudiendo tener una viariación relativamente amplia sin salirse del estandar para aplicaciones especiales.

Los controladores proporcionales e integrales convencionales utilizados para mantener el voltaje de salida del StatCom en condiciones nominales, exhiben un desempeño pobre cuando existen fallas severas en el sistema o la carga, donde la señal de error tiene saltos muy grandes en magnitud. La estrategia utilizada en este trabajo emplea tanto el error como la variación en el mismo para dividir el control en pequeñas secciones, que pueden ser seleccionadas con el uso de reglas simples. Los resultados de simulación muestran la viabilidad de la propuesta de este trabajo y la implementación en un prototipo de laboratorio valida cada parte del dispositivo con resultados experimentales.

Abstract

This dissertation describes the use of the Static Synchronous Compensator (StatCom) in the reactive power compensation and the power quality improvement. The assembling of a Voltage Source Converter (VSC) that meets the IEEE Std 519-1992 (IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems) is emphsized. The low Total Harmonic Distortion (THD) that this VSC produces, allows this power conditioner to be considered for its use on stringent applications. The reinjection principle used, makes this proposal be considered as an affordable solution to the sinusoidal synthesization due to the reduced number of switches needed. The reinjection transformer is one of the most important elements in this configuration, and it can have a wide turn ratio's variation without leading out the special application standards.

The conventional PI controllers applied to maintain the output voltage of the StatCom around nominal conditions exhibit poor performance under severe disturbances, where the error signal jumps with big steps in magnitude. The strategy followed in this research, employs the error and error's variation to break down the control action into smaller sections that can be selected according to simple rules. Simulation results evidence the proposal's suitability, while experimental results validate each part of the device.

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Chapter 1

Introduction

1.1. Background

Deregulation, open access, and cogeneration in electrical power systems are creating transmission congestion scenarios and forced outages. Increasing the number of transmission lines is a non viable solution to these potential problems mainly due to costs and environmental issues. To have efficient and reliable power system operation to develop new control schemes is needed, able to handle dynamic disturbances such as transmission lines tripping, loss of generation, short-circuits, load rejection, while the reactive control has to be fast enough to maintain the desired voltage levels and the system stability. Flexible Alternating Current Transmission System (FACTS) devices have been proposed for fast dynamic control of voltage, impedance, and phase angle in high-voltage ac lines. The application of this technology has opened new and better opportunities for an appropriate transmission and distribution control. The series and shunt power systems compensation are used with the purpose of improving the operating conditions. Respect to the voltage, the compensation has the purpose of handling reactive power to maintain bus voltages close to their nominal values, reduce line currents, and reduce system losses. The voltage magnitude in some buses may be controlled through sophisticated and versatile devices such as the StatCom, which can synthesize the reactive power from small values of storing elements [1.1], and is a power reactive source [1.2][1.3]. By regulation of the StatCom's output voltage magnitude, the reactive power exchanged between the StatCom and the transmission system can be controlled [1.4][1.5][1.6][1.7][1.8].

Since the StatCom may cause interference on the system's fundamental sine wave at frequencies that are multiples of the fundamental one, special care should be paid to ensure not to pollute it,

preventing further harmonic problems. In general, there are three common strategies to construct a VSC minimizing the harmonic content at the output: (*i*) the multipulse; (*ii*) the multilevel; (*iii*) and the pulse-width modulation (PWM) [1.9][1.10].

In the multipulse strategy, the period of the signal is broken down into equal sized parts respect to the pulse number. Switches are triggered once per cycle at the fundamental frequency, and the pulse's amplitude is controlled mainly by the magnetic output stage. The more pulses gives the less output Total Harmonic Distortion (THD).

In the multilevel strategy, the DC source has to be broken down into parts of equal amplitude (x), resulting in a signal of 2x-1 levels. Switches are also switched once per cycle at the fundamental frequency. The output THD depends on the amount of DC sources or divisions available in the DC link.

On the other hand, the PWM strategy uses fast commutations to obtain a low THD, the faster commutations are the lower THD; however, it is limited because of the switches' commutation speed and requires always an output filter to be coupled to the grid.

This research deals with a combination of multipulse and multilevel strategies with emphasis on the use of multipulse configuration in order to reach the minimum total harmonic distortion.

A great deal of methods for stepping-up the number of pulses in the multipulse converters' output has been investigated. The simplest one is by increasing the number of six pulse modules through their corresponding transformers (4 six pulse converters result in 24-pulse, 8 six pulse converters result in 48-pulse operation, and so forth). The weakness of this method is the large size and high cost due to the number of bridges and transformers. Thus, in order to utilize the VSC in special applications such as airports or hospitals, to attain an 84-pulse signal, an array of 14 six pulse modules with 42 transformers is required, besides a huge control task to have a reduced total harmonic distortion (THD), which makes the entire array an impractical solution.

A good strategy to get the 84-pulse waveform by a twelve pulse along with an eight level reinjection converter is presented in [1.10]. The cost is 26 extra switches and 7 DC voltage sources (capacitors) respect to the conventional 12-pulse converter. The control task is hard because of the amount of gate signals needed, and it is prone to unbalance problems due to the large chain of capacitors. Multi Level Voltage Reinjection (MLVR) H-bridge conversion is another option to generate the 84-pulse signal. It requires 5 additional DC voltage sources and 12 switches respect to a conventional 12-pulse converter, but it can be easily used to have more levels in the reinjection by adding H-bridges in series [1.11]. An auxiliary multilevel circuit in the

DC link side has been proposed for reinjection in [1.6]-[1.9][1.12]; it employs fewer components while the THD is bigger than that needed for special applications. This research presents a strategy to generate the 84-pulse VSC, assembled by combining one twelve pulse converter with one seven level converter used as the reinjection scheme. The extra components, respect to the conventional 12-pulse converter, are: 8 switches, 4 DC voltage sources, 4 diodes for the seven level converter, and one reinjection transformer. This amount of components and the wide turn ratio allowed by the reinjection transformer, constitute an attractive array in terms of cost and reduced output voltage total harmonic distortion.

1.2. Motivation

The semiconductors device evolution and digital signal processors development have given rise to the concept of Flexible Alternating Current Transmission Systems (FACTS), with the objective of improving the power system's operating conditions. The operating principle of these devices is simple in nature when we think about supplying the current or voltage needed to have optimum parameters, either on the power system or the load. However, this simple approach vanishes when the general conditions of the grid voltage variations and the load composition and unbalance is taken into account.

The efforts performed all over the world to improve the power quality have originated several power conditioners, which by themselves contribute to power degradation due to switching of the semiconductor devices, and harmonic effects generated in the converters. Thus, big elements have been used as filters, pursuing to have appropriate power quality with low extra noise. Because of that, this technology has not been probed in stringent applications such as hospitals or airports, which are two of the environments to consider.

The main motivation for this work is to analyze a solution to optimize the transmission and power quality, using a strategy able to improve the power quality but limited on the generated harmonic distortion, in order to be applied without large filters. A prototype to probe the strategy has been assembled.

1.3. Justification

The StatCom is a FACTS device with a great deal of attributes, such as quick response in the adjustment of the required output levels, fewer space requirements than other shunt FACTS devices, flexibility, and excellent dynamic characteristics under various operating conditions. Its main objective is to generate an almost harmonic-free and controllable three-phase AC output voltage waveform at the point of common coupling (PCC), to regulate reactive current flows by generating and absorbing controllable reactive power through the solid states switching algorithm [1.13]. This is one of the most widespread devices studied. However, the state-of-the-art review indicates that a high number of switches, magnetic and reactive elements are needed in order to be able to get a low output THD. This research has been proposed taking into account the current technologies and the advantages of each one on the voltage source converters (VSCs) assembling, including the advantages of using the multi level strategies on the synthesis of a staircase signal with a low number of reactive components, but with the low switching speed characteristic of the multipulse converters, and also a low number of magnetic devices. The proposed strategy saves the total amount of switching devices, while proportionates low THD, which is really attractive in special applications.

1.4. Objectives

Equipment that uses FACTS principles is being a viable solution to the problem of reactive power and voltage control in transmission and distribution systems. The StatCom's development has been well reported in literature with its versatile applications in power system. In this research, the StatCom is used with reactive power control purposes, having the following objectives:

☑ To present a novel strategy to attain a reduced output Total Harmonic Distortion (THD) in the Voltage Source Converter (VSC).

☑ To utilize an algorithm for fast synchronization of the StatCom into the electric power system (EPS).

☑ To use a segmented PI controller in the StatCom connected to the (EPS), subjected to several common disturbances in voltage and load levels.

☑ To build a prototype that can be used for further researches.

☑ To provide the needed information to being able to assemble the StatCom.

1.5. Contributions

The major contributions of this research are summarized in the following.

☑ The utilization of the reinjection principle to build the Voltage Source Converter (VSC), demonstrating that by using a seven level converter, along with a transformer with a non-stringent turn ratio, a reduced output Total Harmonic Distortion (THD), may be reached. A study of the reinjection transformer's turn ratio has been done to justify the performance of our proposition respect to the THD indicated in the IEEE Std. 519.

☑ The digital Phase Loocked Loop (PLL) synchronization scheme has been tested, showing that it does not need a zero crossing detection routine of the main three phase voltage to synchronize the gating control signals.

☑ The verification of the synchronization scheme in the StatCom prototype. This is an important point in order to save effort and time within the designing stage.

☑ The utilization of a control scheme called segmented PI controller for the StatCom connected to the (EPS), which illustrates that the big efforts needed to keep the complete system stable after severe disturbances, are reduced when the total system control stage is broken down.

☑ The assembling of a prototype.

1.6. Thesis structure

This dissertation is composed by 4 chapters.

Chapter 1. Presents introductory material along with the motivation and objectives of this research.

Chapter 2. Illustrates the followed strategy to attain the proposed 84-pulse VSC topology and its interaction with the grid system when it is used as StatCom.

Chapter 3. Reveals how the control stage is broken down in order to have better dynamic performance in the whole system, and proves through simulations the response to several common disturbances.

Chapter 4. Details through experiments the reached results.

Appendix A. Shows a list of publications stemming from the developed work.

Appendix B. Gives general information about the VSC assembling.

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Chapter 2

84-pulses StatCom

2.1. Introduction

The StatCom is a power electronic-based Synchronous Voltage Generator (SVG) able to provide fast and continuous capacitive and inductive reactive power supply. It generates a three-phase voltage, synchronized with the transmission voltage, from a DC energy source, and it is connected to the EPS by a coupling transformer. The regulation of the StatCom's output voltage magnitude gives rise to the reactive power exchange between the StatCom and the transmission system. The StatCom's basic structure illustrated on Fig. 2.1 consists of a step-down transformer, a three-phase voltage source converter (VSC), and a DC capacitor [1.1]-[1.6].

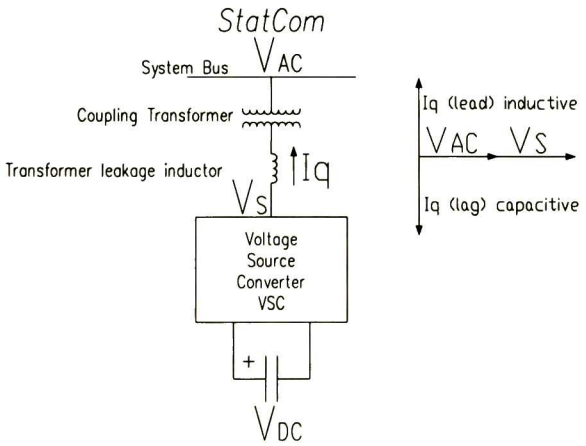

Fig. 2.1 StatCom's Basic Structure

This chapter is focused on the internal structure of the proposed VSC to get a low THD output voltage. Likewise, the main aspects to connect the StatCom to the grid are reviewed.

2.2. Reinjection Configuration

There are three main strategies to build a VSC: (*i*) the multipulse; (*ii*) the multilevel; (*iii*) and the pulse width modulation (PWM)[2.7][2.8].

In the multipulse strategy, the period of the signal is broken down into equal sized parts in relation to the pulse number. The switches are triggered once per cycle at the fundamental frequency, and the amplitude on each pulse is controlled mainly by the output magnetic stage. The more pulses produces the less output Total Harmonic Distortion (THD).

In the multilevel strategy, the DC source has to be broken down into parts of equal amplitude (x), given rise to a 2x-1 levels signal. Switches commute once per cycle at the fundamental frequency. The THD depends on the amount of DC sources or divisions available in the DC link.

On the other hand, the PWM technique uses fast commutations to reach a low THD. The faster commutations are, the lower THD. However, it is limited due to the commutation speed of the switches and requires always an output filter coupled to the grid. This research deals with a combination of the first two strategies with emphasis on the use of multipulse configuration in order to reach the minimum total harmonic distortion.

There is a difference on the twelve pulse converter used in this work, respect to the standard twelve pulse converter. The DC source is not common to both six-pulse modules. In this proposition, a positive multipulse signal between the main terminals of the first six pulse converter and another positive multipulse signal with opposite phase between the main terminals of the second six pulse converter are connected. In order to have a neutral point, the negative of the first converter is connected to the positive of the second converter, Fig. 2.2.

Each branch in the six pulse converters must generate electrical signals with 120° of displacement between them; the upper switch is conducting while the lower one is open and vice versa (180° voltage source operation) [2.9].

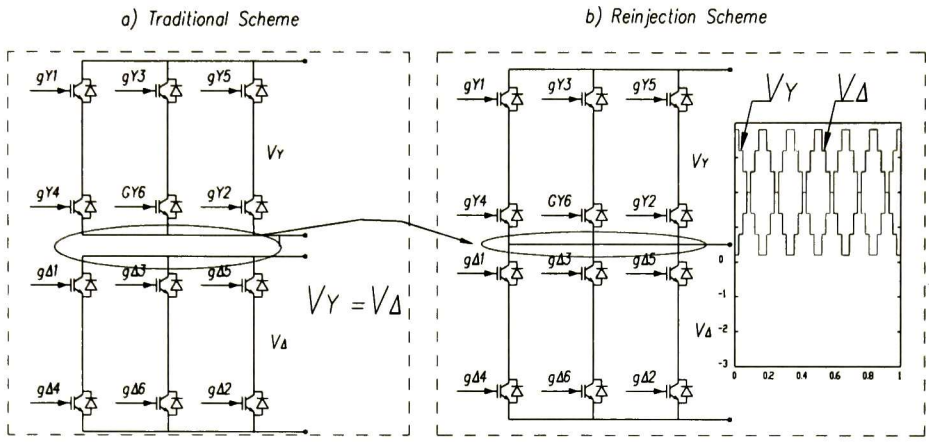

Fig. 2.2 a) 12 pulse Traditional Scheme, b) 12 pulse Reinjection Scheme fed by a 7 level converter.

A 30° displacement in the firing sequence of both converters must be considered. Transformer's turn ratios are 1:1 and $1:\sqrt{3}$ on the YY and YΔ transformers, respectively. In order to operate the VSC in special applications such as airports or hospitals, in this research a 84 level voltage signal is proposed, generated through a 7 level auxiliary circuit operating as a re-injection scheme. The auxiliary circuit is common to the three phases, reducing the number of extra components. The topology to provide the pulse multiplication is detailed in [2.7][2.8][2.10]-[2.13], and illustrated in Fig. 2.3.

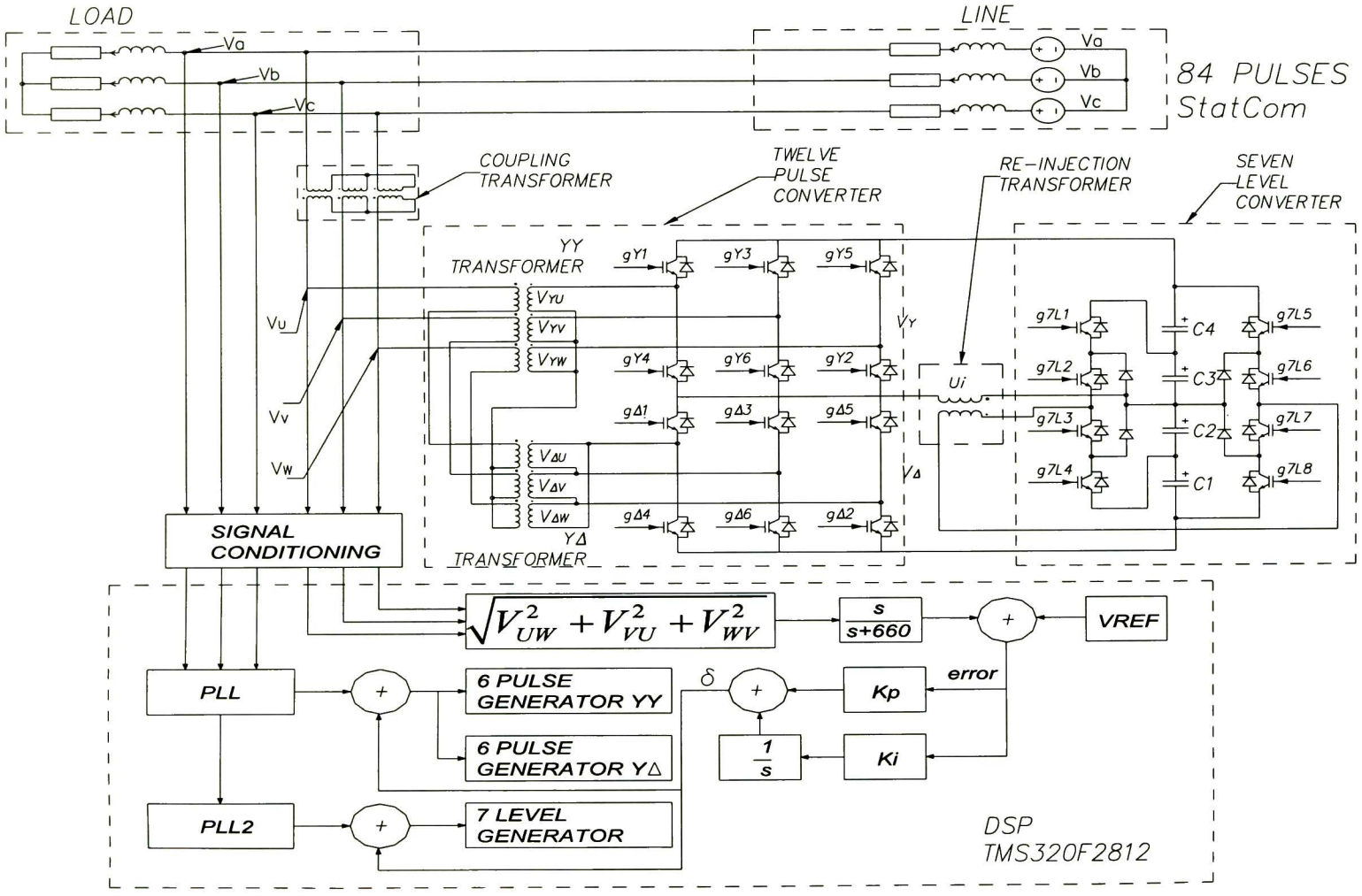

Fig. 2.3 84-pulse StatCom structure

2.3. Total Harmonic Distortion

In order to apply the seven level inverter output voltage to feed the standard twelve pulse converter, special care should be paid to not inject negative voltage into V_Y or V_Δ; notice the inclusion of the injection transformer between both arrays. Thus, input voltages in the six pulse converter may be regulated by adjusting the injection voltage U_i by:

$$V_Y = V_{DC} + U_i \tag{1}$$

$$V_\Delta = V_{DC} - U_i \tag{2}$$

The injection voltage is determined by the seven level inverter switching pattern and the injection transformer turns ratio. When voltages V_Y and V_Δ are used as inputs to the six pulse converters, a cleaner VSC output voltage comes about. Fig. 2.4. exhibits the followed strategy to generate V_{YU} and $V_{\Delta U}$ as the interaction of the seven level output and the corresponding six pulse signals. These signals have been obtained from an electrical simulation developed in PLECS®, within MATLAB/Simulink environment.

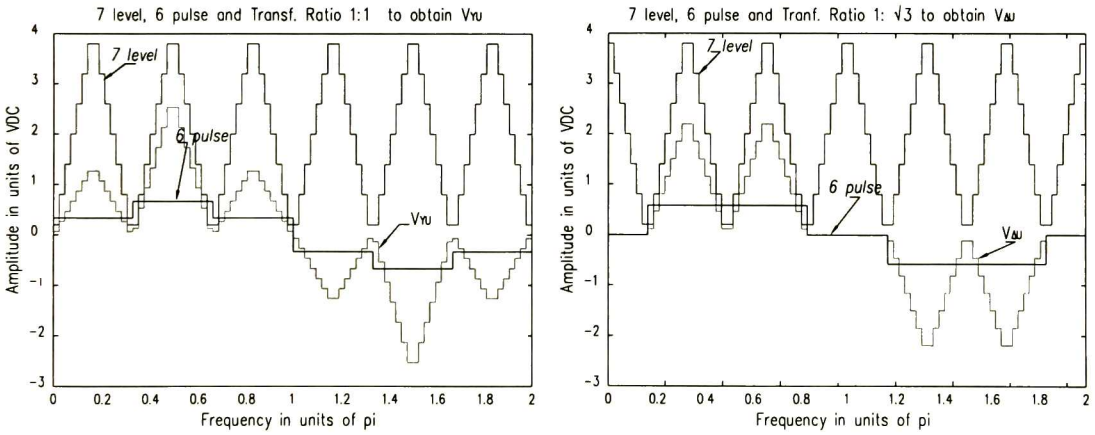

Fig. 2.4 Mixing seven level, six pulse signals, and transformer ratios to attain V_{YU} and $V_{\Delta U}$.

Through the 1:1 ratio in the *YY* TRANSFORMER, and $1:\sqrt{3}$ for the *Y*Δ TRANSFORMER, adding their corresponding output signals, the 84-pulses line-to-neutral signal VU emerges, with the harmonic spectrum in Fig. 2.5 (linear scale) and in Fig. 2.6 (logarithmic scale).

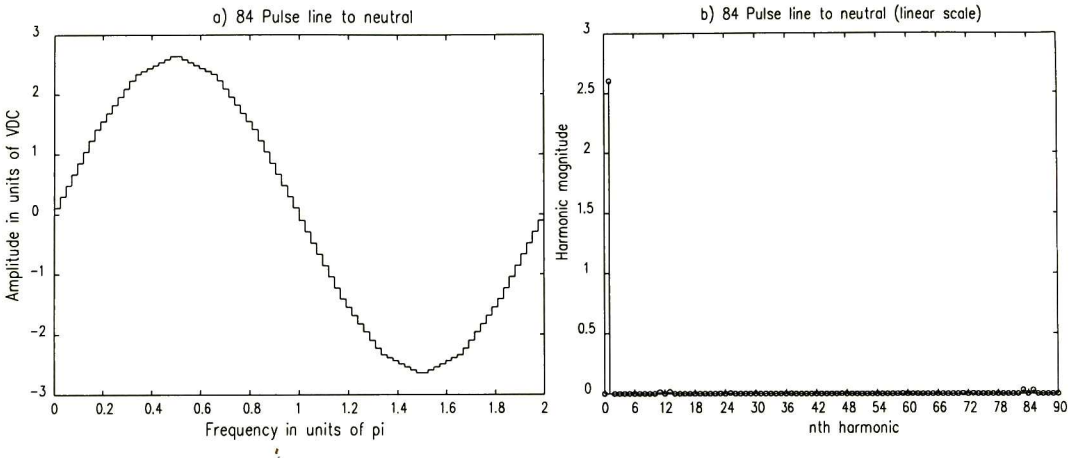

Fig. 2.5 84-pulses line-to-neutral output voltage and harmonic content (linear scale)

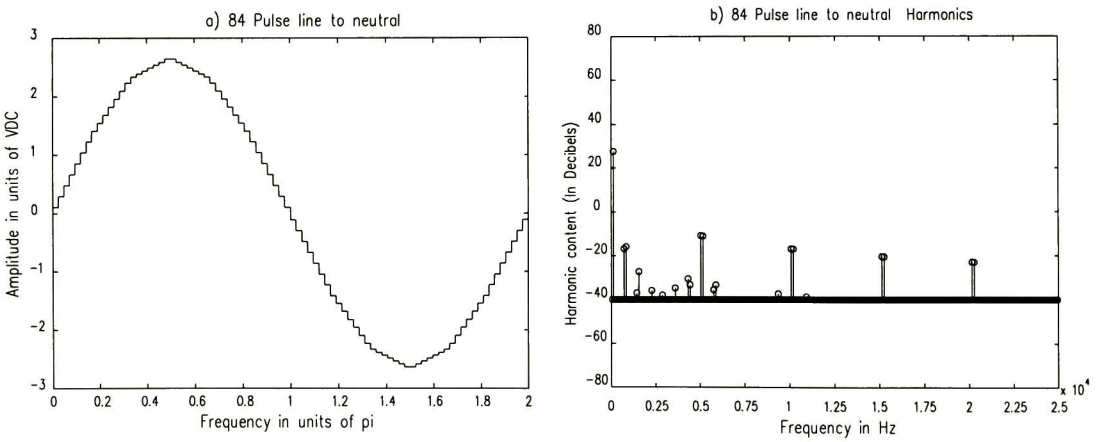

Fig. 2.6 84-pulses line-to-neutral output voltage and harmonic content (logarithmic scale)

The StatCom's phase voltage VU is an odd symmetric signal, so that the Fourier's even terms become zero. Thus,

$$V_U(t) = \sum_{n=1}^{\infty} V_{U_{2n-1}} \sin\left((2n-1)\omega t\right) \tag{3}$$

$$V_{U_{2n-1}} = \frac{4V}{3\pi(2n-1)}\left(A_{2n-1} + aB_{2n-1}\right) \tag{4}$$

$$A_{2n-1} = 2 + 2\cos\left(\frac{1}{3}\pi(2n-1)\right) + 2\sqrt{3}\cos\left(\frac{1}{6}\pi(2n-1)\right) \tag{5}$$

$$B_{2n-1} = \sum_{i=0}^{20} Coeff_i \cos\left(\frac{i}{42}\pi(2n-1)\right) \tag{6}$$

$$Coeff = \begin{Bmatrix} -3, & 1, & 1, & 1, & 1, & 1, & 1,\ldots \\ -3\sqrt{3}, & \sqrt{3}-1, & \sqrt{3}-1, & \sqrt{3}-1, & \sqrt{3}-1, & \sqrt{3}-1, & \sqrt{3}-1,\ldots \\ -3, & -\sqrt{3}+2, & -\sqrt{3}+2, & -\sqrt{3}+2, & -\sqrt{3}+2, & -\sqrt{3}+2, & -\sqrt{3}+2 \end{Bmatrix} \tag{7}$$

being a the re-injection transformer's turns ratio.

The 84-pulse signal value (VU) depends on the injection transformer turns ratio a, which is determined in order to minimize the THD, defined by [2.7][2.14]

$$THD_{VU} = \sqrt{\frac{\sum_{n=2}^{\infty} V_{Un}^2}{V_{U1}^2}} \tag{8}$$

The minimization of THD yields the parameter a. In this research such calculation has been carried out in MATLAB with n = 7200, and increments $\Delta a = 0.0001$. With these parameters, the minimum THD becomes 2.358% with $a = 0.5609$, value employed on the previous figures.

The distortion limits according to the IEEE Std. 519 indicate that the allowed THD in voltage is 10% in dedicated systems, 5% in general systems, and 3% for special applications as hospitals and airports [2.14].

Table 2-1 presents the minimum THD in the output voltage produced with several multipulse configurations. The THD produced through this proposition allows its use even in applications with stringent quality requirements; it exhibits less dependence to variations on the transformer's turns ratio a, which can have variations until ±12.5% to get a maximum THD lower than 3%. This means that a strict reinjection transformer's turn ratio is not needed to get a THD within a stringent condition. Fig. 2.7 illustrates the dependence of the THD respect to variations in the re-injection transformer's turn ratio a. All these values had been obtained using MATLAB.

Table 2-1 Minimum THD produced through the multipulse VSC

Number of pulses	THD (%)
12	15.22
24	7.38
48	3.8
60	3.159
84	2.358

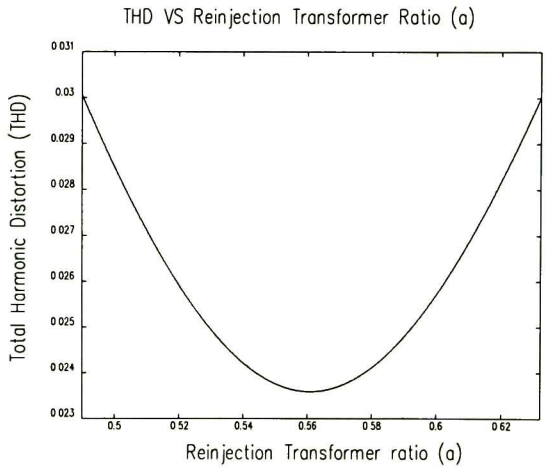

Fig. 2.7 Dependence of the THD respect to the reinjection transformer's turn ratio

2.4. StatCom's arrangement

Connecting the improved VSC to the system for reactive compensation requires several points to be taken into account. This section deals with such details using Fig. 2.3 as the main scheme, including a coupling transformer 13.8 kV : 13.8 kV, and considering the following transmission line parameters, at 75°C :

- Conductor code name: Grosbeak Aluminum Conductor Composite Core (ACCC)
- Voltage rating: 13.8kV peak
- Resistance: 0.0839 Ω/ km
- Inductive Reactance: 0.2574 Ω / km
- Line length: 50km
- Load Resistance: 202.5 Ω
- Load Inductive Reactance: 0.6H

If we pursue to eliminate the active power exchange between the StatCom and the system, the DC voltage sources are replaced by capacitors.

Secondly, it must be ensured that the StatCom's frequency and phase angle are equal to the system ones; these parameters will be obtained by using a novel synchronizing arrangement able to detect instantaneously the phase angle. The seven level inverter must switch at six times the frequency of the six pulse converters to ensure phase and frequency.

The digital signal processor (DSP)-control implementation must take the voltage levels needed for the ADC (analog/digital converter) to detect the signals with appropriate precision, and must refresh the output data before to take new samples in order to be considered real time. It is also needed to provide isolation from the power stage.

2.4.1. Synchronization of signals

The Phase-Locked-Loop (PLL) is the synchronizing circuit responsible for the determination of the system's frequency and phase-angle of the fundamental positive sequence voltage of the controlled AC bus [2.15]. The PLL utilizes the Stationary Reference Frame in order to reduce computational costs, and helps to improve the system's dynamic performance [2.16]. Digital PLL is an algorithm able to detect the fundamental component of the phase-voltages, synchronizing the output signal to the frequency and phase of the input one. This algorithm does not require a

zero crossing detection routine for the input voltage or the generation of internal reference signals for the input current [2.17]. The PLL strategy used employs a $-\tan^{-1}\left(\alpha/\beta\right)$ function added to a correction value determined by the signs of α and β, Fig. 2.8.

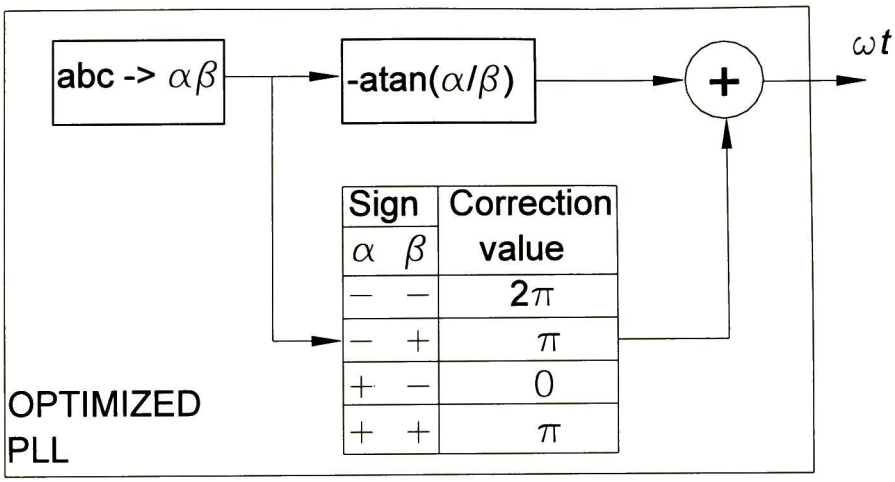

Fig. 2.8 PLL Strategy

This block synchronizes the PLL's zero output respect to the startup of the α signal, when the β signal presents its minimum value, Fig. 2.9.

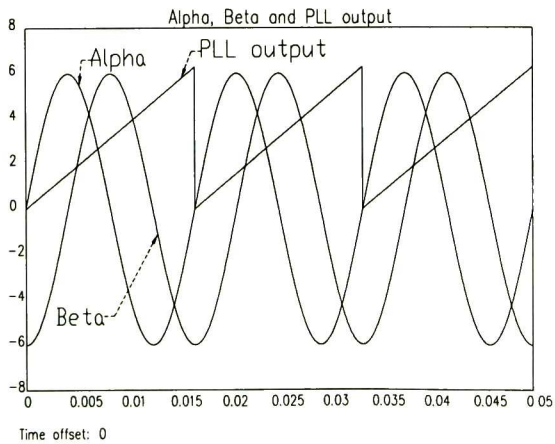

Fig. 2.9 α, β, and PLL-output

2.4.2. Firing sequence

The second block is the six pulse generator, which is responsible to generate the pulse sequence to fire the three-phase IGBT array. It consists of an array of six pulse spaced 60° each other. In this block, the IGBT will operate at full 180° for the *on* period, and 180° for the *off* period. Any disturbance in the frequency will be captured by the synchronizing block, preventing errors. The falling border in the synchronizing block output signal is added to a series of six 60° spaced signals that would be sent to the opto-coupler block gate, which will feed each six pulse converter. The *off* sequence turns out in a similar way but waiting 180° to keep the same duration *on* and *off* in each IGBT, Fig. 2.10.

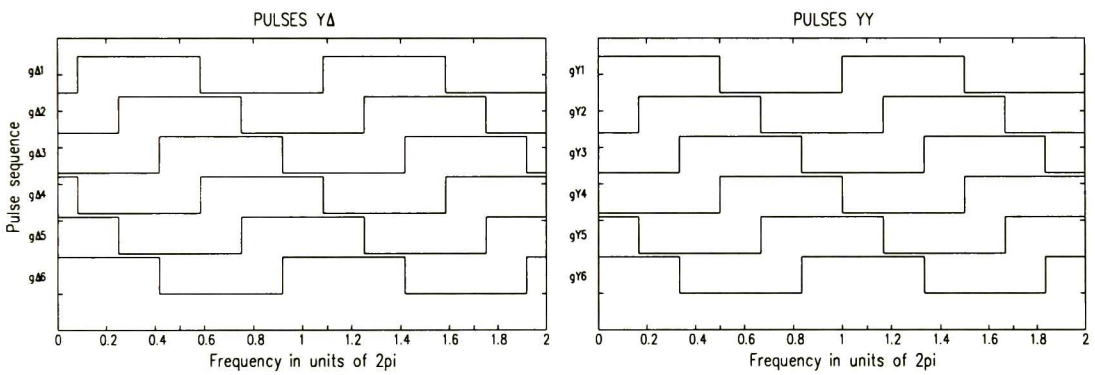

Fig. 2.10 Firing sequence for the six pulses modules

2.4.3. Seven level generator

In order to produce the pulse sequence needed to generate the seven level inverter, six times the frequency of the six pulse generator should be ensured beginning at the same time. This is achieved by monitoring the falling border in the novel PLL output signal, and using it along with the modulus operator with the $\pi/3$ argument. This signal will be the period for the seven level generator, which will modify its state each $\pi/42$ rad. Fig. 2.11 depicts the asymmetric pulse

sequence for such seven level inverter, along with the seven level voltage for a complete sinusoidal cycle and a $\pi/3$ zoom-in, in order to observe the detailed pulse signals.

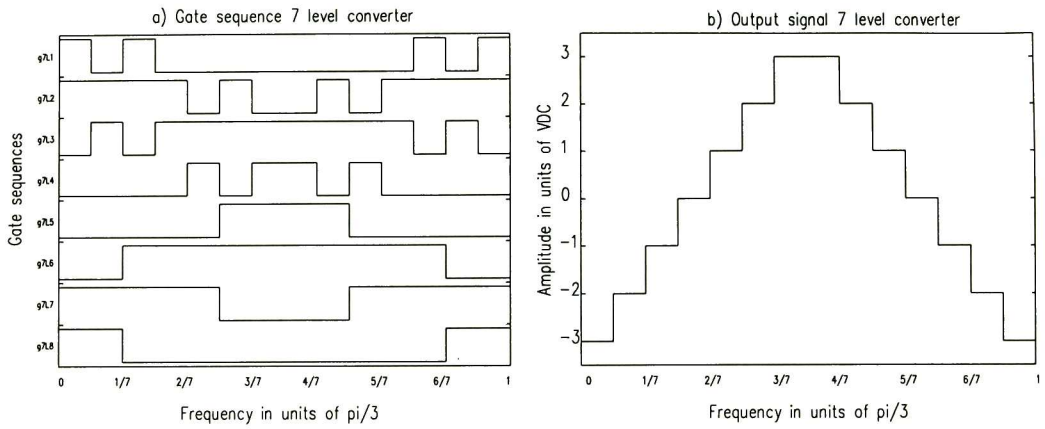

Fig. 2.11 Seven level gate signals

2.4.4. Angle's Control Circuit

The reactive power exchange between the AC system and the compensator is controlled by varying the fundamental component magnitude of the inverter voltage, above and below the AC system level. The compensator control is achieved by small variations in the semiconductor devices' switching angle, so that the fundamental component of the voltage generated by the inverter is forced to lag or lead the AC system voltage by a few degrees. This causes active power to flow into or out of the inverter, modifying the value of the DC capacitor voltage, and consequently the magnitude of the inverter terminal voltage, and the resultant reactive power [2.6]. The angle's control block diagram is described in [2.16] for a PI controller, and depicted in Fig. 2.12. The inputs are the line-to-line voltages of the controlled AC bus prior to the coupling transformer. The reference voltage VREF is chosen as the RMS value for a pure sinusoidal three phase signal, which is $\sqrt{1.5}$ times the peak of the line voltage. This value is compared to the filtered RMS StatCom voltage output (VRMS) multiplied by the coupling transformer's turn ratio; it may contain an oscillating component. The output signal δ corresponds to the displacement angle of the generated multipulse voltage, with respect to the controlled AC bus voltage (primary voltage of the converter transformer). The low-pass-filter (LPF) is tuned to

remove the characteristic harmonic content in the multipulse configuration; for the twelve pulse it begins with the 11th harmonic. The PI controller has a limiting factor by dividing the error signal by the reference voltage VREF in order to have the δ signal with a maximum value of -1 when the StatCom output is equal to zero. In the following chapter special attention is paid to the fuzzy segmented PI controller.

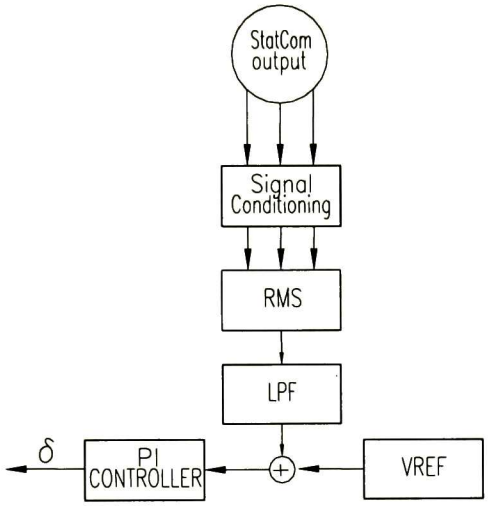

Fig. 2.12 StatCom's power angle control

2.5. Chapter References

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Chapter 3

Control Strategy

3.1. Introduction

Conventional PI or PID regulators have been applied to control the StatCom's output voltage around nominal conditions or subject to disturb like voltage unbalance [3.1]-[3.4]. Such controllers may exhibit poor performance under other disturbances, where the error signal jumps with big steps in magnitude. In this research, it is desireable to find a controller that can deal with most of the problems detailed in [3.5]. The strategy followed employs the error and error's variation to break down the control action in smaller sections that can be selected according to simple rules.

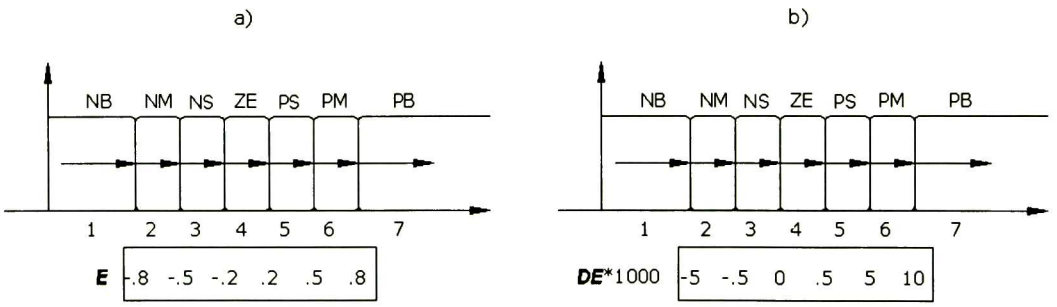
3.2. Segmented PI controller

The complete system presented on Fig. 2.3 was tested under several disturbances using a PI controller tunned for steady state operation. Special attention was paid to measure the error and estimate the error's increment when the disturbances were applied. It was verified that a motor startup is a quite demanding situation to test the StatCom's performance, so it was used to define the membership function limits. For simplicity on the controller design, crisp membership functions were used to describe seven linguistic variables similarly to the fuzzy set notation as follows:

- ☑ NB→ negative big,
- ☑ NM→negative medium,
- ☑ NS→negative small,
- ☑ Z→zero,
- ☑ PS→positive small,
- ☑ PM→positive medium,
- ☑ PB→and positive big.

Fig. 3.1a) displays the error signal, which varies from -1 to +1, and Fig. 3.1b) displays the variation on the error signal. This variation was estimated using MATLAB ode23t solver with variable step. The error (*e*) and its variation (*de*) are represented by lowercase as the independent variables; they are continuous values. The uppercase represents the fuzzy set obtained by selecting the indicated membership functions limits.

Fuzzy control rules are usually obtained empirically. This dissertation uses the rules presented in [3.6] to define the zones of the segmented PI, Table 3-1.



$$E = \begin{cases} NB & -\infty < e \le -.8 \\ NM & -.8 < e \le -.5 \\ NS & -.5 < e \le -.2 \\ ZE & -.2 < e \le .2 \\ PS & .2 < e \le .5 \\ PM & .5 < e \le .8 \\ PB & .8 < e \le \infty \end{cases} \qquad DE*1000 = \begin{cases} NB & -\infty < de \le -5 \\ NM & -5 < de \le -.5 \\ NS & -.5 < de \le 0 \\ ZE & 0 < de \le .5 \\ PS & .5 < de \le 5 \\ PM & 5 < de \_ 10 \\ PB & 10 < de \_ \infty \end{cases}$$

Fig. 3.1 Membership functions

Table 3-1 Control rules

DE / E	NB	NM	NS	ZE	PS	PM	PB
NB	1	1	1	2	3	3	4
NM	1	2	2	2	3	4	5
NS	1	2	3	3	4	5	6
ZE	1	2	3	4	5	6	7
PS	2	3	4	5	5	6	7
PM	3	4	5	6	6	6	7
PB	4	5	6	7	7	7	7

The strategy to tune the segmented PI zones is summarized in the following steps.

1. Tune up a conventional PI at steady state. The proportional and integral gains obtained were: $K_P = 0.5411$, and $K_I = 20.3718$. Such values were used on the segmented PI controller as the starting point, preserving the same gain values in the seven zones. Thus, firstly the conventional PI and the segmented PI controllers are equivalent.
2. Taking into account that capacitors are used in the DC link in order to the system operates as StatCom, initially without charge, according to section 2.4.4 the maximum error is -1. It is convenient to adjust the gains' value zone 1 due to it corresponds to the biggest negative error and the biggest negative error's variation. To adjust the values of this zone, we must maintain K_P as low as possible to keep the system stable. Then, reduce K_I to the value that allows less oscillation in the segmented PI sections. After this step, zone 1 would have the values for the biggest negative error and error's variation, and the other zones the original steady state values.
3. Starting up an induction motor when the capacitors are fully charged is considered one of the most demanding situations and is used for adjusting the remaining zones. To tune the gains of segment 2, use the value of K_P as low as possible to keep the system stable. Then,

reduce K_I to the value that allows less oscillation in the zones presented on the right and low corner of Fig. 3.5.

4. Repeat step 3 for sections 3, 5, 6, and 7 in sequence. This will bring up to the segmented PI, Table 3-2. After tuning up the seven zones, the output will be between zones 3 and 4 on steady state.

Table 3-2 Gain values of the segmented PI

Fuzzy Rule	Kp	Ki
1	0.5252	5.0929
2	0.5411	38.9929
3	0.5570	40.7436
4	0.5729	40.7436
5	0.5570	20.3718
6	0.4933	20.3718
7	0.3183	40.7436

It is important to note that using a different disturbance, the values would vary slightly, but this was the most demanding condition.

3.3. Simulation Results

The StatCom model and the segmented PI controller with the values obtained from the previous section were simulated in MATLAB/Simulink, using Piece-wise Linear Electrical Circuit Simulation (PLECS). PLECS was used because it is a fast simulation toolbox for electrical circuits within the Simulink environment specially designed for power electronics systems. It is also a powerful tool for any combined simulation of electrical circuits and controls [3.7]. The PLL-block feeds the two six pulse generators at the fundamental frequency and it is used to bring forth the seven level pulses at six times the fundamental frequency to have them synchronized to the system and configured as the 84-pulse StatCom. The δ signal calculated

from the segmented PI controller is utilized to lag or lead the StatCom voltage respect to the system. While the phase-angle lags the bus voltage ($\delta < 0$), energy is flowing to the DC capacitor, charging it and doing the StatCom draws capacitive current. Contrarily, inductive current is drawn while ($\delta > 0$) [3.8]. The figures 3.2 to 3.5 illustrate the system behavior when short-duration root-mean-square (rms) problems [3.9] are presented.

A sag or dip is a reduction of AC voltage at a given frequency lasting from 0.5 cycles to 30 cycles and magnitudes between 0.1 to 0.9 pu, it is usually caused by system faults, and is often the result of switching on loads with heavy startup currents [3.5][3.9]. Fig. 3.2 exhibits the system behavior when a sag of 6 cycles and 0.3 pu appears in the system. Using a conventional PI controlled StatCom the error has several oscillations as presented in Fig. 3.2a; Fig. 3.2b is the error when a segmented PI controlled StatCom is employed. The smoother and faster behavior of this new controller becomes visible. Fig. 3.2c-d are included to illustrate the rules corresponding to each error and error's increment. The conventional PI controller used the original values and this is presented as rule number 4.

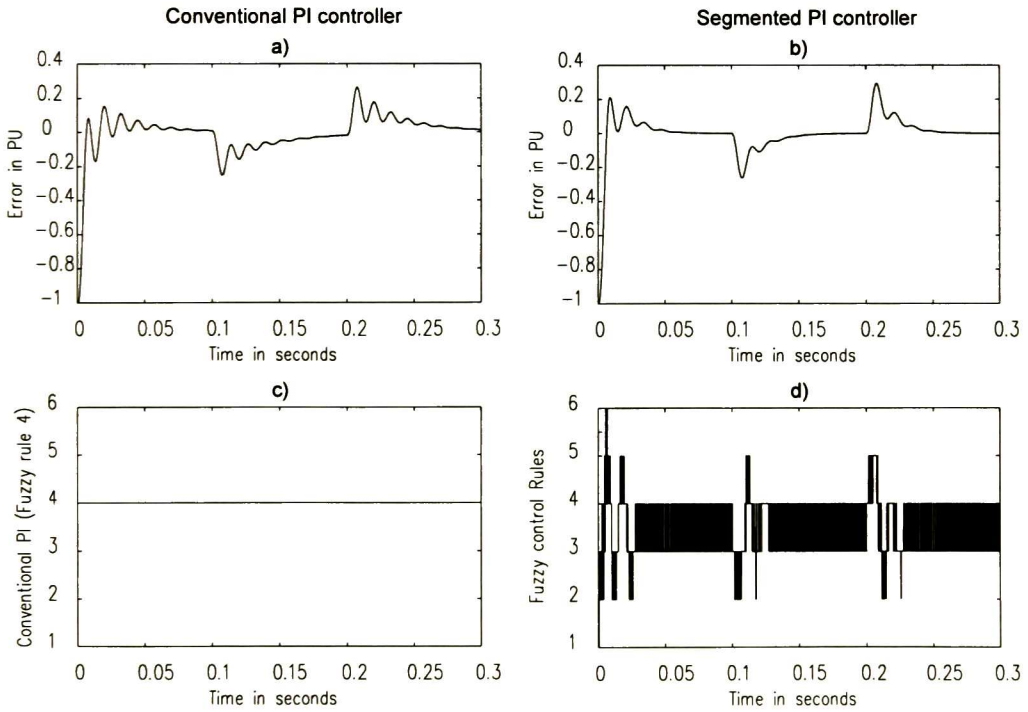


Fig. 3.2 Sag 0.3 PU

Contrarily to a sag, a swell represents an increase in the AC voltage, lasting from 0.5 cycles to 30 cycles and magnitudes between 1.1 to 1.8 pu. Swells commonly arise due to high-impedance neutral connections, sudden (especially large) load reductions, and a single-phase fault on a three-phase system [3.5][3.9]. Fig. 3.3 presents the system under a swell of 6 cycles and 0.3 pu. It can be noticed that Fig. 3.3a presents more oscillation than Fig. 3.3b. Also the steady state is reached faster using the segmented PI controlled StatCom. Again, Fig. 3.3c-d are included to illustrate the rules corresponding to each error and the error's increment, using original values in rule number 4 for the conventional PI controller.

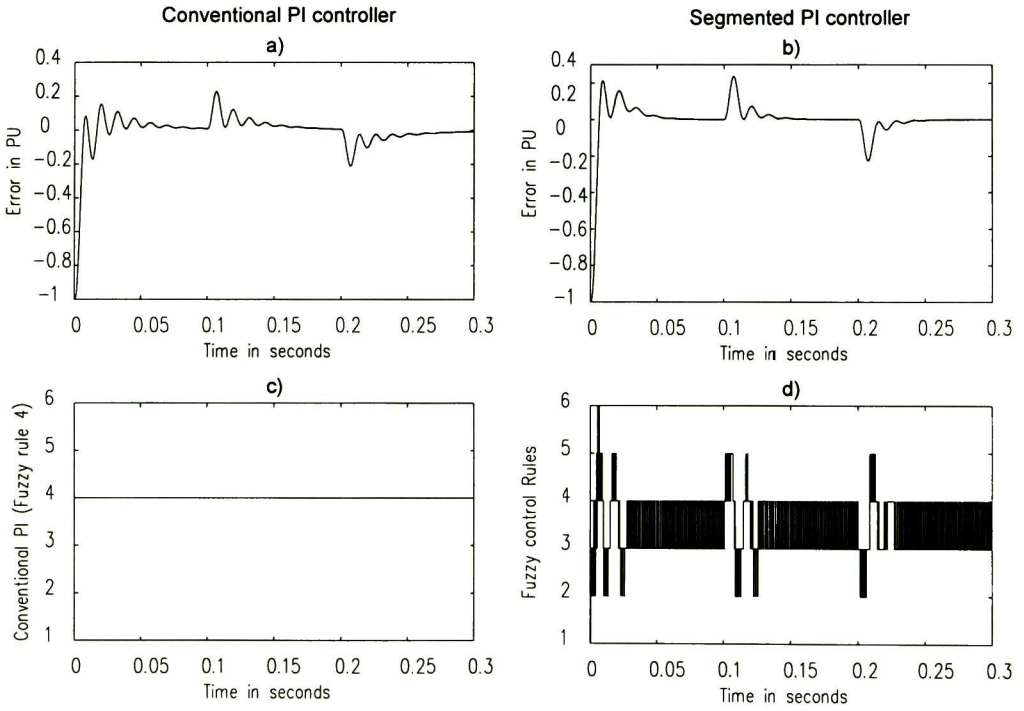


Fig. 3.3 Swell 0.3 PU

An interruption occurs when the supply voltage or load current decreases to less than 0.1 pu for a period of time not exceeding 1 min. Interruptions can be the result of power system faults, equipment or control failures. An interruption, whether it is instantaneous, momentary, temporary, or sustained, can cause disruption, damage, and downtime, from the home user up to the industrial user, and it can cause equipment damage, ruination of product, as well as the cost associated with downtime, cleanup, and restart [3.5][3.9]. Fig 3.4 illustrates the controllers' error

behavior after a 3 cycles three-phase fault at the load bus. The error is defined as the difference between the measured voltage and the reference voltage; the greatest error becomes -1 while the fault is *on*, but, once this one is released, the error is bigger than 1 pu with a conventional PI, Fig. 3.4a. In contrast, the segmented PI presents an error around 0.4 pu, Fig. 3.4b. Notice the oscillations in the conventional PI response, while they are smoothed with the use of the segmented controller. Fig. 3.4c-d are included to illustrate rule number 4 for the conventional PI controller, and the rules of the segmented PI, respectively.

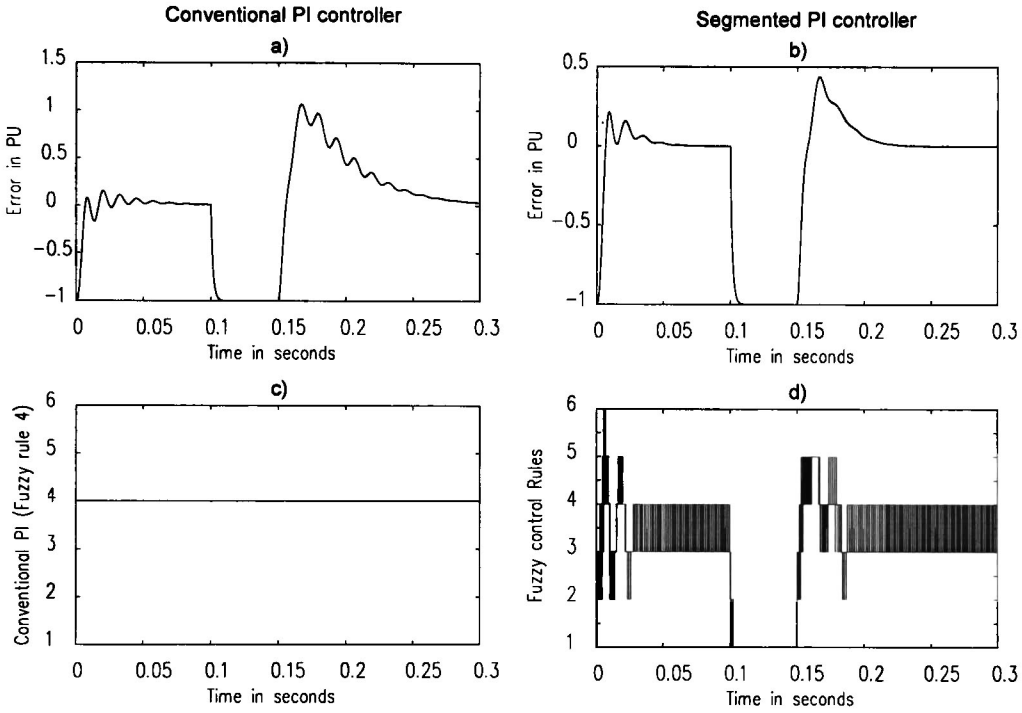


Fig. 3.4 Three-Phase Failure

Oscillatory transients and voltage fluctuation commonly arise when a motor is connected. At this point, a sudden change in the steady-state condition of a signal's voltage, current, or both is performed and a series of random changes in magnitude and frequency is presented. A single PI is not as fast as needed to get a smooth startup. Fig. 3.5 depicts the behavior of the error when a motor load is started.

The parameters of the induction motor are the following:

☑ 2250HP (2300V),

- ☑ Rs = 0.029 Ohms,
- ☑ Lls = 0.0006 Henries,
- ☑ Rr = .022 Ohms,
- ☑ Llr = 0.0006 Henries,
- ☑ Lm = 0.0346 Henries,
- ☑ J= 6.5107 Joules.

The error for the conventional PI has several big oscillations, Fig. 3.5a, while the segmented one exhibits very fast response to reach the steady state, and minimum oscillation, Fig. 3.5b. Fig. 3.5c-d are also included to illustrate the rule number 4 (conventional PI controller), and the rules of the segmented PI, respectively.

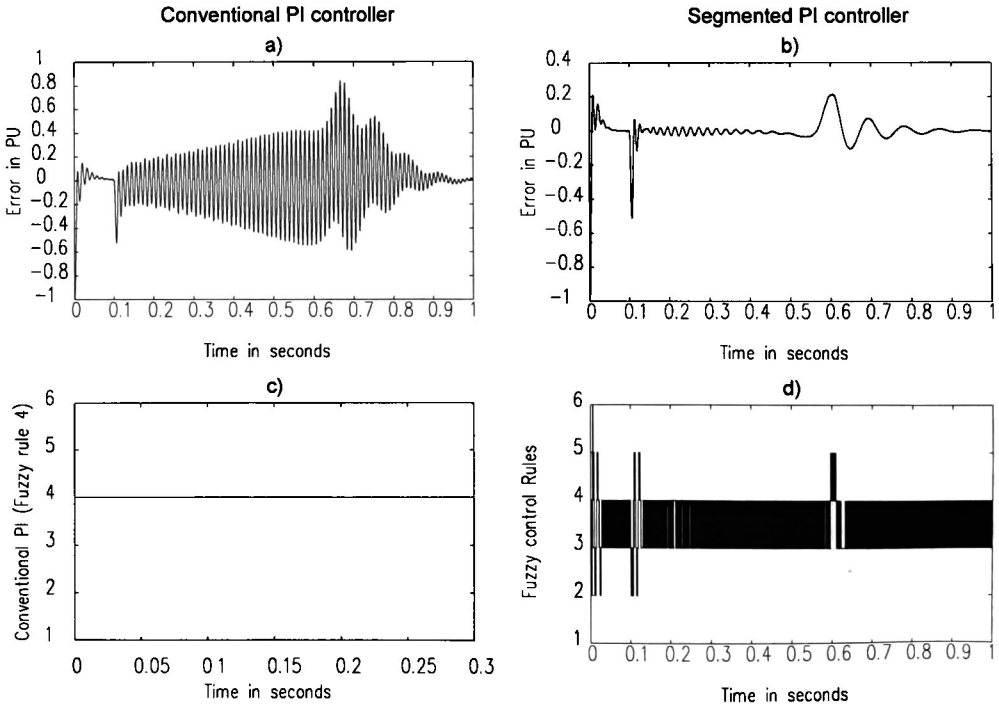


Fig. 3.5 Motor Start up

With these simulations it is demonstrated that when the system is stressed, the segmented PI controller exhibits a quite appropriate response.

3.4. Chapter References

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Chapter 4

Experimental results

4.1. Introduction

Previous chapters have described the complete VSC's structure as a StatCom, or in special applications along with the controller's configuration. In this chapter, results on the prototype are displayed through images coming from oscilloscope that validate each part of the device. These images are referred to previous sections for comparison between theoretical and practical data. These experimental results are exhibited as they were collected from the prototype, by increasing the complexity of the whole circuit. Important is to consider the nomenclature used, variables with subscripts a, b, or c, represent the source side, while variables with subscripts U, V, or W, are for the StatCom output. When it is needed to differentiate both sides on the transmission line, subscripts a, b, or c are used, indicating if the source node or the load node is referred. The structure of this chapter is the following: Section 4.2 presents the 84 pulse VSC output, indicating the harmonic content. Section 4.3 demonstrates the behavior of the PLL for voltage synchronization and break down into the three phases for connecting the StatCom to the grid. Section 4.4 presents the open-loop characteristics of a multipulse StatCom connected to the grid, which uses DC voltage sources on the DC link, in comparison to the StatCom connected to the grid but using capacitors on the DC link, Section 4.5. The implementation of a PI controller for voltage tracking is presented on section 4.6. Section 4.7 presents a special case when the balance on the load is lost, and finally, Section 4.8 gives some conclusions of the experimental results obtained on this research.

4.2. VSC based on multipulse strategy

All the images presented in this section were captured with a Tektronix® TDS2024B oscilloscope which has only one reference point for the four acquired signals. Fig. 4.1 reveals the line-to-line voltage V_{UV} and V_{UW} of a twelve pulse VSC output (without connection to the grid), and illustrates that the twelve pulse converter output modified according to Fig. 2.2 exhibits exactly the same characteristics than a conventional twelve pulse converter when both input voltages (V_Y and V_Δ) of equal magnitude are used.

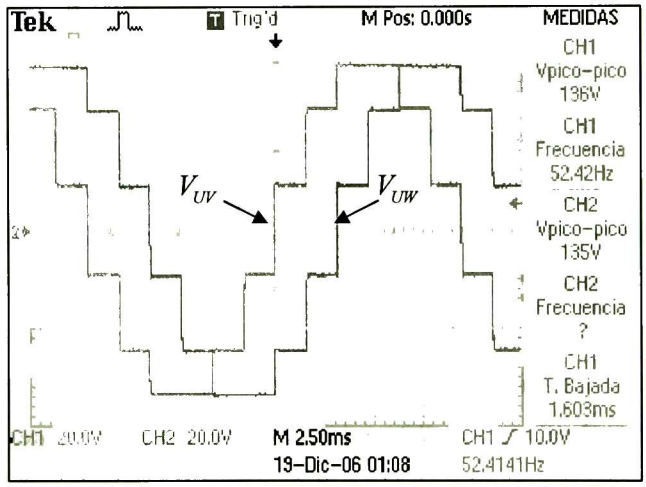

Fig. 4.1 Conventional twelve pulse output voltages

Fig. 4.2 presents the single-phase seven level inverter output (U_i, equations (1)-(2), chapter 2). This is the needed signal at the input of the reinjection transformer, which output would be added to a continuous DC value in order to get V_Y and V_Δ according to Fig. 2.2 (chapter 2). This signal has six times the system's frequency, which is needed to have a complete cycle for each pulse on the six pulse converters output. The zero crossing of this signal must match with each three-phase zero-crossing.

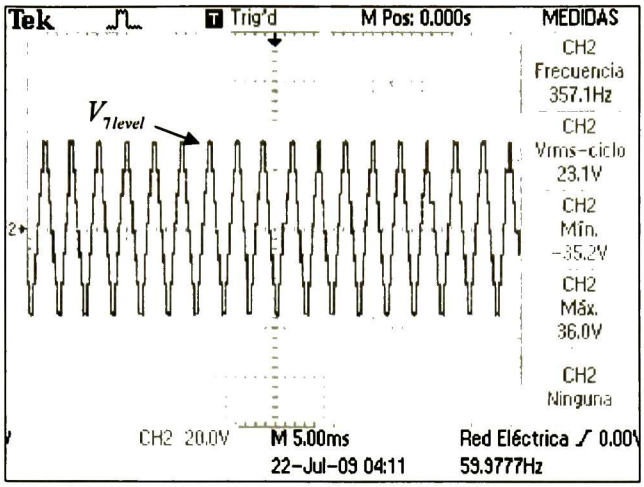

Fig. 4.2 Seven level converter output

In order to validate the strategy to build V_{YU} and $V_{\Delta U}$ Fig 2.3 of chapter 2 is used as reference. The seven level converter output, Fig. 4.2, is passed through the reinjection transformer connected as a step-down transformer; the transformer output U_i is added to the voltage of capacitors C_4 and C_3 to build V_Y, and C2 and C_1 to build V_Δ. Voltage V_{DC} used in equations (1)-(2) of chapter 2, corresponds to the voltage in capacitors C_4 and C_3, or C_2 and C_1. Using voltages V_Y and V_Δ as the inputs to the six pulse converters, and measuring after transformers YY and YΔ, the VSC's outputs are those displayed in Fig. 4.3 and Fig. 4.4. These signals correspond to the ones illustrated in Fig. 2.4, chapter 2.

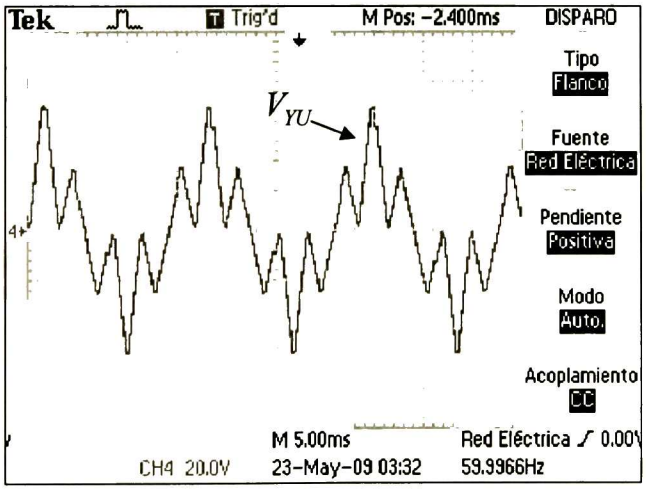

Fig. 4.3 V_{YU} built when the seven level signal is injected into the six pulses converter with (YY-transformer)

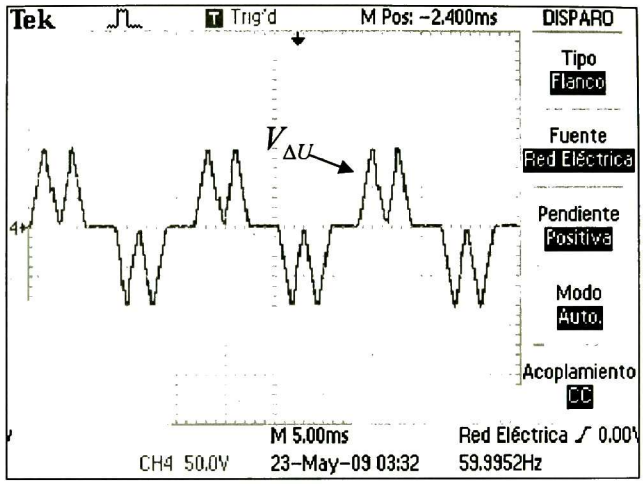

Fig. 4.4 $V_{\Delta U}$ built when the seven level signal is injected into the six pulses converter (YΔ-transformer)

Fig. 4.5 verifies that by adding the voltages in Fig. 4.4 and Fig. 4.3, the resultant waveform has the desired shape. The harmonic content is presented in Fig. 4.6. It was gotten with a Hanning window on the Tektronix® TDS2024B oscilloscope. There are significant magnitude harmonics each about 5 kHz, which corresponds to the number $84r \pm 1 \quad r = 0,1,2...$ when we use a 60 Hz signal. These harmonics are concurrent to the traditional multipulse harmonic content.

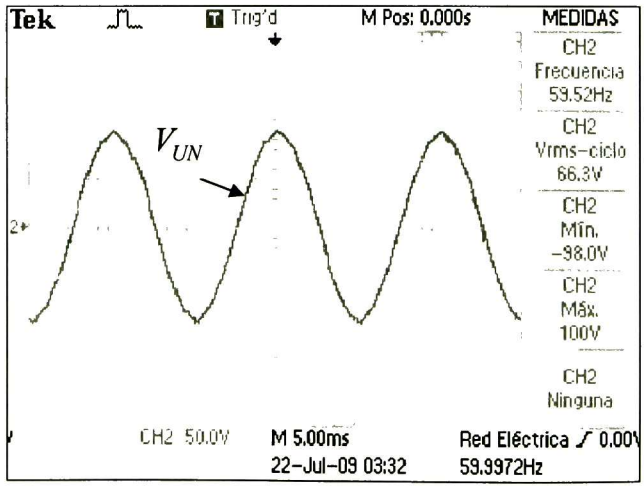

Fig. 4.5 84-pulses signal obtained through the combination of V_{YU} and $V_{\Delta U}$

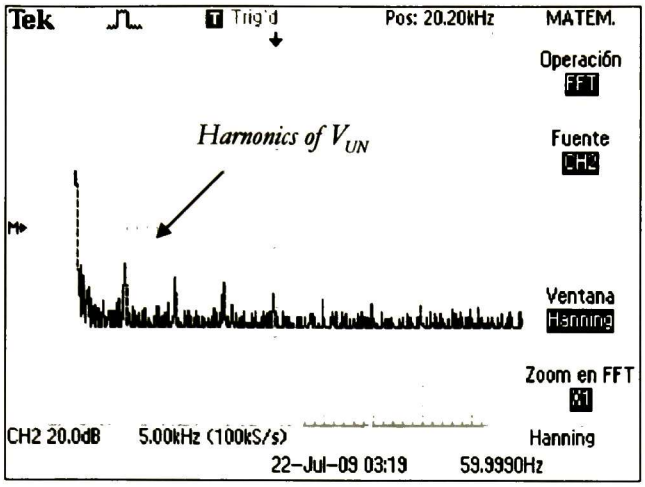

Fig. 4.6 84-pulses output signal's harmonic content.

4.3. StatCom Synchronized to the grid

All the images presented in the following were captured using a Tektronix® TPS2024 oscilloscope with four isolated channels. The Phase-Locked-Loop (PLL) is the element responsible to determine the system's frequency and the fundamental signal's phase-angle. In order to verify its usefulness, Fig. 4.7 depicts the VSC's line-voltage output respect to the grid line voltage. The waveform, phase, and output frequency, demonstrate the system's ability to track the input, and the PLL's effectiveness.

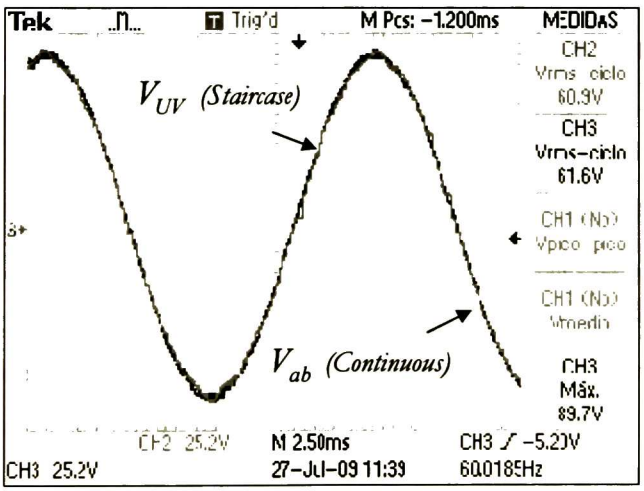

Fig. 4.7 VSC's output voltage synchronized in phase, frequency, and amplitude

Fig. 4.8 displays the three-phase line-to-line voltages arisen from the VSC. It can be noticed that the angle difference among phases is 120°, as needed in a three-phase signal. The frequency of these signals is equal to that of the grid.

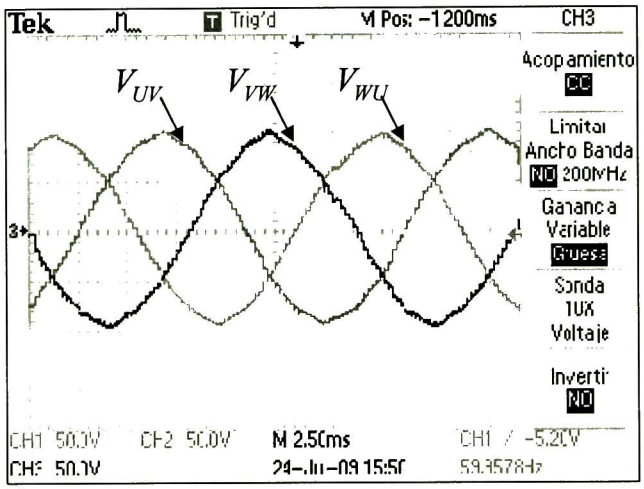

Fig. 4.8 Three phase 84-pulses VSC output

4.4. StatCom based on energy storage

The use of an energy storage device, such as a bank of batteries, becomes quite important to verify the system's behavior in the case of using DC renewable sources or battery storage to provide active power capabilities to the system [4.1] [4.2]. However, due to the use of the DC source some effects that must be taken into account arise. They are summarized in this section.

4.4.1. Notching

If we use a conventional twelve pulse StatCom, the resulting voltage signal would present small disturbances in each pulse level change; these disturbances are termed notching [4.5]. The allowed notching limit according to the IEEE Std. 519 in special applications as hospitals and airports is 10% [4.6]. This limit is exceeded by using a twelve-pulse converter, especially around the zero crossing, Fig. 4.9.

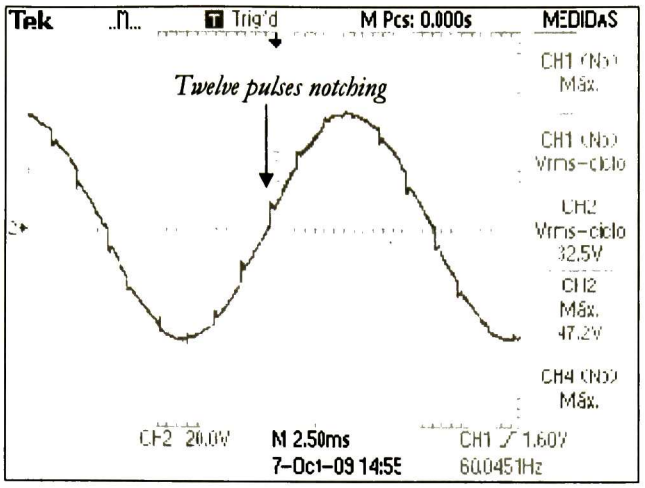

Fig. 4.9 Notching produced by the 12-pulses StatCom based on energy source.

The notching effect can be considerably reduced if the amount of pulses per cycle is increased. Fig. 4.10 illustrates the reduced effect of notching when the 84-pulses StatCom based on energy storage is employed.

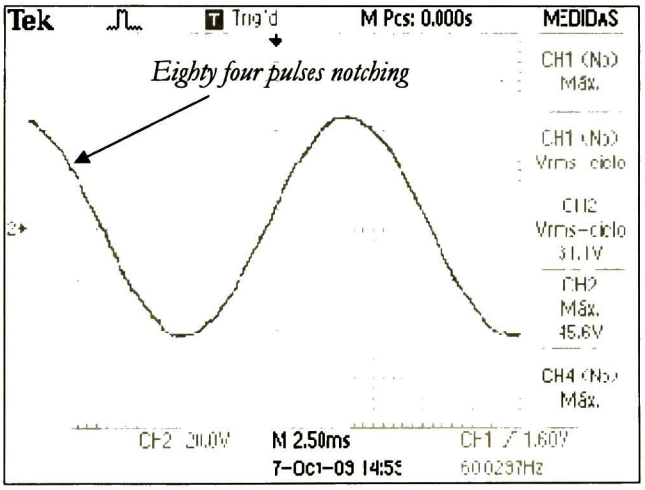

Fig. 4.10 The presence of notching is reduced by the 84-pulses StatCom with energy source.

4.4.2. Harmonics

The following figures were captured when the StatCom based on energy storage is synchronized and connected to the grid. They illustrate one phase of the system, assuming that the behavior is similar in the two remaining phases.

Harmonic distortion is the polution of the fundamental sine wave at frequencies that are multiples of the fundamental. In order to illustrate the harmonic mitigation obtained with the device proposed in this research when DC voltage sources are included on de DC link, the Fig. 4.11 is included, depicting the phase voltage V_{aDSP} passed through the signal conditioning board, which is fed into the eZdsp™ TMS320F2812. This voltage is responsible of the synchronization. The VSC's output, prior to the coupling transformer is also included as $V_U\,(StatCom)$. The load voltage is presented as $V_a\,(Load)$; it is almost twice the $V_U\,(StatCom)$ amplitude. These three signals have the same phase and frequency as the power system requires.

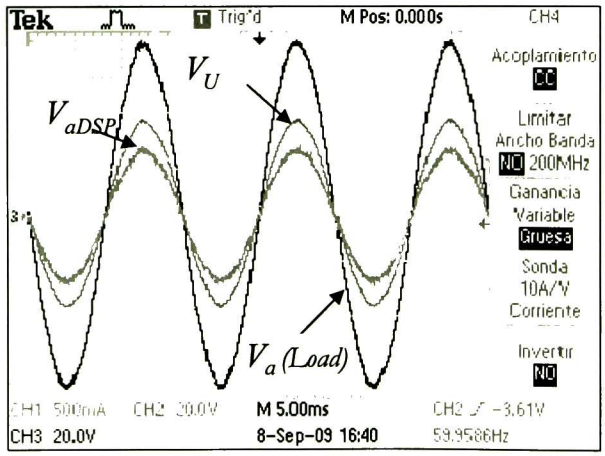

Fig. 4.11 (*i*) Voltage *a* fed into the DSP(V_{aDSP}); (*ii*) StatCom's output voltage U(V_U); (*iii*) load voltage of phase *a* (V_a *(Load)*).

The $V_a(Load)$ Fourier's spectrum, when the StatCom is disconnected from the grid, is illustrated in Fig. 4.12. The spectrum is calculated in the Tektronix® TPS2024 oscilloscope and a Rectangular window, which is commonly used for signals without discontinuities.

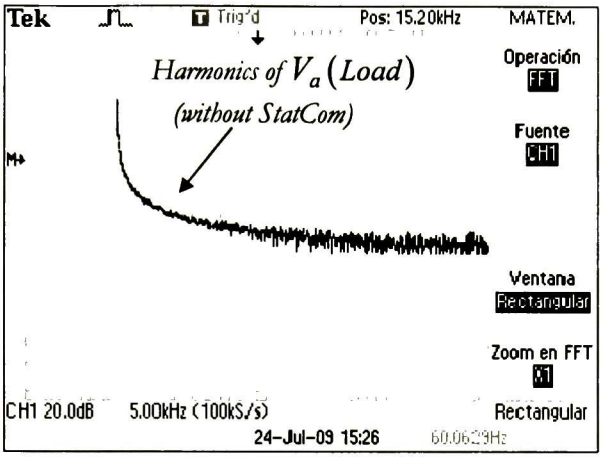

Fig. 4.12 Load voltage Fourier's spectrum without StatCom

Fig. 4.13 depicts the spectrum of $V_a(Load)$ when the StatCom based on energy storage is connected. In this case, small amplitude harmonics are repeated each 5 kHz. Rectangular window for the Fourier's spectrum was used with the objective of being able to compare the spectrums with Fig. 4.13 and whitout StatCom Fig. 4.12.

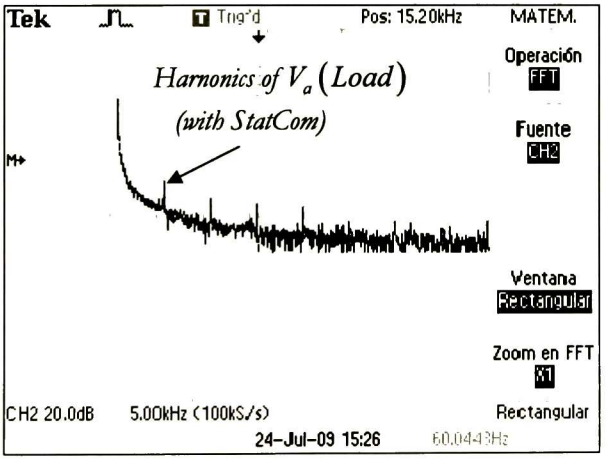

Fig. 4.13 Load voltage Fourier's spectrum with the StatCom based on energy source.

4.5. StatCom with capacitors in the DC-link

In order to use the voltage source converter (VSC) as a reactive power compensator, the voltage sources in the DC link have to be replaced by capacitors. This subsection presents the StatCom behavior when twelve and eighty four pulses are tested.

4.5.1. Twelve-pulse StatCom based on capacitors

Fig. 4.14 displays the StatCom's output voltage (V_U), along with the input voltages V_Y and V_Δ, when the StatCom is connected as a twelve-pulse converter in a neutral point configuration. Voltage V_Y is the addition of voltages across C4 and C3, while V_Δ is the voltage across C2 and C1 (Fig 2.3, chapter 2). With this connection, the seven level converter is disabled. A slight imbalance on V_Y and V_Δ is noticeable. This uneven voltage level is not presented on the simulations with a single capacitor for V_Y and a single capacitor for V_Δ, but it is one of the main problems of multilevel converters, and it must be taken into account when the number of capacitors is increased to have a DC-link multilevel scheme. This problem must be dealt with in a future research.

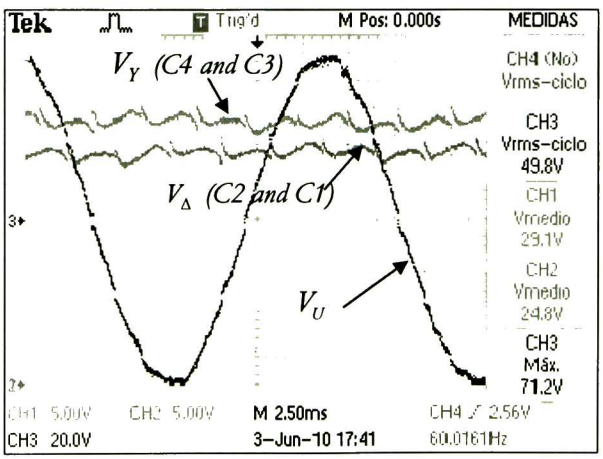

Fig. 4.14 Capacitor voltage for the 12-pulse system

4.5.2. 84-pulses StatCom based on capacitors

Fig. 4.15 illustrates voltage $V_a(Source)$ and voltage $V_a(Load)$ when the 84-pulses StatCom is connected in a neutral point configuration without control loop, adding a RL load constituted by 161.29 ohm and 0.8 henry (Lab-Volt ® 8321-02) per phase. The signal is synchronized in frequency and phase; a slight difference on the amplitude appears due to transmission line components used on the prototype, which has 5.6 Ω and 25 mH per line.

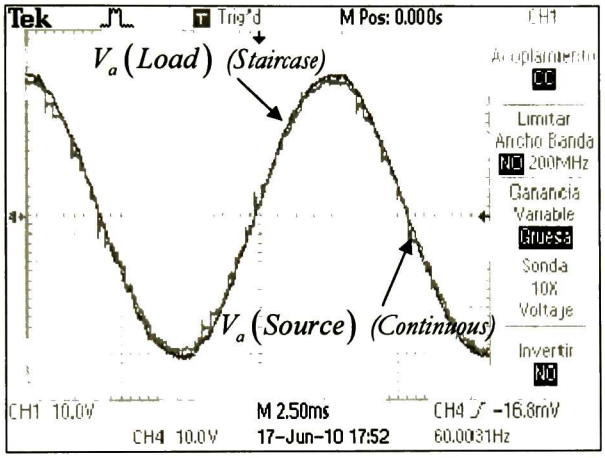

Fig. 4.15 Source and load voltages for the 84-pulse StatCom connected to the grid.

4.6. StatCom reference voltage tracking through a PI controller

Once the StatCom is connected to the grid, it is important to include a controller to verify its performance under some common variations. The StatCom's main objective is to maintain the voltage level on the load bus. Thus, the controller's reference voltage is the magnitude of the voltage needed on the load, and has to be compared with the measured magnitude. A detailed explanation of the StatCom operation is found at [4.7]. Referring to Fig 2.3 (chapter 2), the δ signal used on the pulse generators inside the DSP TMS320F2812 block, represents the phase displacement between the StatCom and the grid. It is responsible for increasing or decreasing the StatCom voltage. Through the appropriate δ selection, a conventional proportional-integral controller has been chosen and configured to have a losses' steady state compensation due to the

transmission line parameters. This PI controller has been assembled in the DSP TMS320F2812 using the bilinear transformation to validate its behavior. The Fig. 4.16 shows voltage $V_a(Source)$ and voltage $V_a(Load)$ for the cases of *low* reference voltage. In this case, $V_a(Load)$ has the frequency and phase-angle corresponding to the $V_a(Source)$, but smaller magnitude. Capacitors were utilized for energy storage.

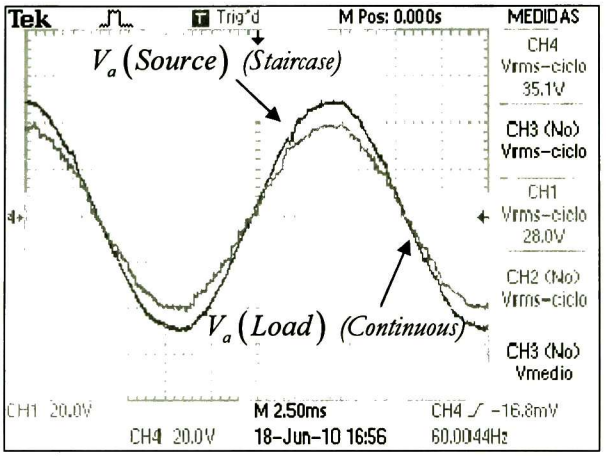

Fig. 4.16 Load voltage when the reference voltage is lower than the source voltage

Fig. 4.17, presents the case with *nominal* reference voltage. In this case, the $V_a(Load)$ has the frequency, the phase-angle, and the amplitude of the $V_a(Source)$, illustrating that the PI controller is able to command the line losses. This is the StatCom's normal operating condition in steady state.

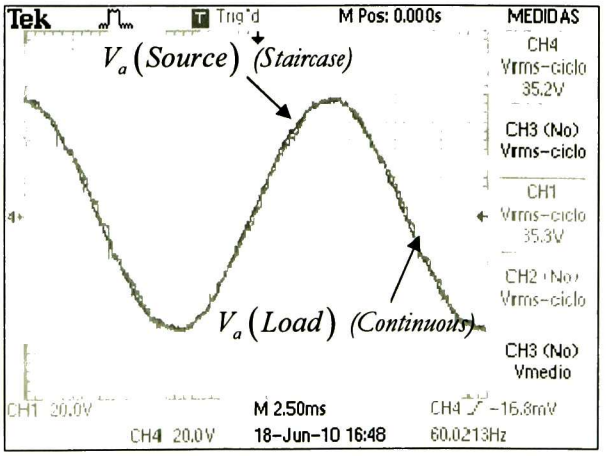

Fig. 4.17 Load voltage when the reference voltage is equal to the source voltage

Fig. 4.18 illustrates the case of *high* reference voltage. It is noticeable that the load voltage can be adjusted to that of the corresponding reference, although the influence of the twelve-pulse converter becomes more evident when Vref is higher than Vsource. A more robust controller is needed to respond appropiatelly to commands in load's higher voltage. The segmented PI controller proposed on this research demonstrates, via simulation, its ability to track low/high reference voltage.

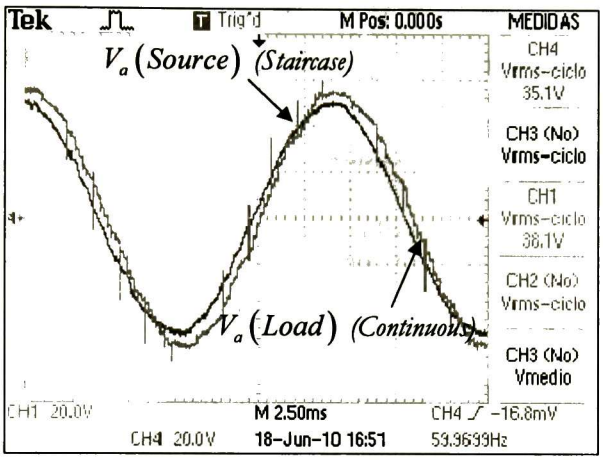

Fig. 4.18 Load voltage when the reference voltage is higher than the source voltage

4.7. Load imbalance

Several researches have been made in order to use the StatCom for source or load imbalance compensation [4.8][4.9][4.10]. Fig. 4.19 displays some signals when a resistive load is used; phase-B in the load is in open-circuit to give rise to a load imbalance. The StatCom is disconnected. Signal $V_a(Source)$ is phase-A voltage. Signal $V_a(Load)$ is the load voltage. It is worth noting the difference in amplitude and phase. The load current $I_a(Load)$ is in-phase with the load voltage due to the resistive load. Signal $P_a(Load)$ represents the instantaneous power on the load.

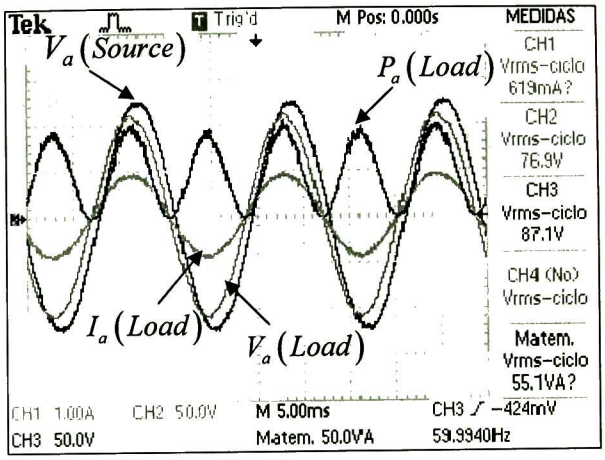

Fig. 4.19 System with resistive load and StatCom disconnected.

Fig. 4.20 demonstrates the usefulness of connecting a StatCom based on energy storage to the previous system. Signal $V_a(Source)$ is the phase-A voltage. Signal $V_a(Load)$ is the load voltage. Their overlapping is due to their same magnitude and phase. The load current $I_a(Load)$ becomes in phase with the load voltage, as a consequence of the resistive load. The $P_a(Load)$ signal represents the instantaneous power drawn in the load. A bigger power sent to the load is evident. The StatCom is not designed to deal with unbalanced conditions. Using energy storage, active power can be used to solve unbalancing problems. Such condition needs separate controllers for each StatCom's phase.

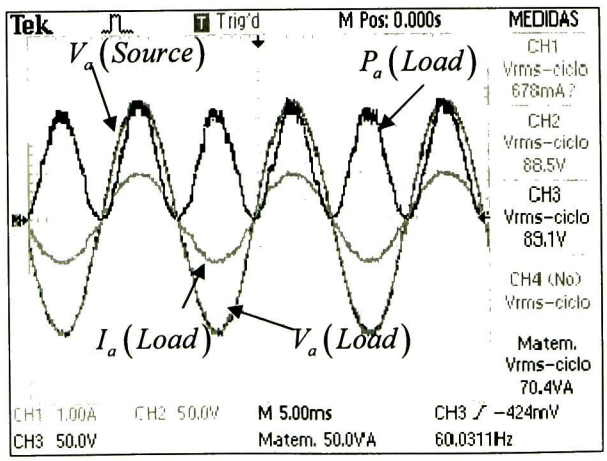

Fig. 4.20 System with resistive load and the StatCom based on energy storage

4.8. Chapter Conclusions

This chapter presents through experimental results, the suitability of this research. Relevant characteristics are sumarized in the following.

- In order to save in switches and capacitors to build a voltage source converter, the reinjection via neutral point can be used, providing a substantial Total Harmonic Distortion reduction.
- The synchronizing scheme (PLL) allows the VSC to be connected to the grid that exhibits fast and continuous voltage magnitude control through the signal δ.
- The PI controller allows the StatCom to compensate losses due to line parameters. Likewise, the controller allows the StatCom to track the reference voltage.
- The use of a large chain of capacitors in the DC-link brings the problem of capacitor's unbalance, which might cause problems after disturbances.
- The StatCom is not designed to operate under unbalanced load conditions. However, by using energy source in the DC-link and independent controllers for each phase, the unbalanced conditions can be temporarily managed.

4.9. Chapter References

[4.1] Z. Yang, C. Shen, L. Zang, M. L. Crow, and S. Aticitty, "Integration of a STATCOM and Battery Energy Storage," IEEE Transaction on power system to Appear.

[4.2] L. Zang, C. Shen, M. L. Crow, "A Comparison of FACTS Integrated with Battery Energy Storage System", IEEE 2001.

[4.3] Static Synchronous Compensator (STATCOM) with Energy Storage Pallavi Mahale, K.D.Joshi, Electrical Engineering Department, G.H.Raisoni College of Engineering, Nagpur, INDIA

[4.4] A DC-DC Multilevel Boost Converter, Rosas-Caro, J.C.; Ramirez, J.M.; Peng, F.Z.; Valderrabano,A.; Power Electronics, IET Volume 3, Issue 1, January 2010 Page(s):129 – 137. Digital Object Identifier 10.1049/iet-pel.2008.0253

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[4.7] Davalos-Marin, R.: 'Detailed Analysis of a multi-pulse StatCom', Cinvestav – Internal Report. May 2003, http://www.dispositivosfacts.com.mx/dir_tesis_doc.html.

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[4.9] Tsai, S.-J.S.; Yun Chang; "Dynamic and unbalance voltage compensation using STATCOM", Power and Energy Society General Meeting Conversion and Delivery of Electrical Energy in the 21st Century, 2008 IEEE, Issue: 20-24 July 2008,pp 1 – 8.

[4.10] S. Dong, L. Wenhua, and W. Zhonghong, "Study on the operation performance of STATCOM under unbalanced and distorted system voltage," in Power Engineering Society Winter Meeting, 2000. IEEE, 2000, pp. 2630-2635 vol.4.

Conclusions and further work

General Conclusions

This dissertation presents a study about one of the most used VSC-based FACTS devices: the StatCom.

A novel strategy to generate higher pulse number by combining one twelve pulse converter with a seven level converter, in order to attain the overall 84-pulses VSC performance with the corresponding high quality voltage wave, has been presented. The associated seven level converter is built through the combination of two three level topologies with asymmetric gate pattern inverters. The explanation of the control stages is described.

Through simulations and experimental results, the suitability of the proposal is demonstrated. The reinjection principle, mainly applicable with Total Harmonic Distortion reduction purposes, has been demonstrated utilizing the harmonics' calculation. With this low THD, the inverter is able to be used in special applications. The proposition allows savings in the total amount of employed switches along with a small quantity of capacitors to prevent problems of umbalancing.

The 84-pulses VSC physical implementation, synchronized in phase, frequency, and amplitude has been succesfully accomplished. The PLL allows the StatCom to be right away synchronized to the grid within a sample cycle. The employed angle's control induces the possibility to draw variable reactive current from the system. Capacitive current drawing increases the controlled AC bus voltage amplitude, while inductive current drawing decreases the AC voltage, producing a

very fast dynamic response under reference voltage variations, even with the use of a very simple control scheme.

The use of a segmented PI controller allows the appropriate StatCom's response, even under large disturbances in the bus and the load. Simulations depict the transient behavior under severe conditions, revealing that the system can be used even on this type of stringent situations. This represents a good alternative for the device's control.

The device performance, proven on a lab prototype, allows verify the harmonic content of the resultant voltage signal.

Further Work

The 84-pulses VSC physical assembling synchronized in phase, frequency, and amplitude has been succesfully accomplished. Important is to take into account that the voltage sources should be changed by a capacitor chain in order to have reactive power exchange only. This change in energy storage elements would conduct to uneven charge and discharge of the capacitors. It is recommended to use an improved voltage balance scheme.

It is of big importance to have the complete system able to be used in new researches, this means to have a friendly module available. VSC communications with computer are important and a change on the DSK should be considered due that eZdsp™ TMS320F2812 is flashed using parallel port of computers, which is not present on new desktop and laptop computers.

DSP implementation is limited to the VSC control and PLL implementation along with a single PI controller scheme. The resources used within the DSP allow the segmented PI controller to be implemented on the same device. The closed loop and a single PI controller have been implemented with good results. Important is also to consider that slight modifications should be done to the source code to adapt it to a new DSK. The eZdsp™ F28335 board is suggested since it belongs to the same family and the code modification would be negligible, and communication through USB port is available.

The control stage on this work used crisp membership functions as rules. It is important to use some other membership functions to probe efectiveness of the proposal.

Tha study of the StatCom under unbalaced conditions is a primary issue.

Appendix A

Publications

This section presents the publications that have resulted from this research.

A.1. **Unidad Convertidora De Voltaje De 84 Pulsos Para Aplicaciones Especiales,** AntonioValderrábano González, Juan M anuel Ramí rez, Francisco Beltrán Carbajal, IEEE XII Reunión de Otoño de Potencia, Electrónica y Computación, ROPEC'2010.

A.2. **A Fuzzy Control for Power Electronic-Based Devices.-** Valderrábano, A.; Ramirez, J.M.; Power Symposium, 2010. NAPS 2010. 42th North American 26-28 Sept. 2010.

A.3. **Modern control of a multi-level DC voltage reinjection VSC.-** Valderrábano, A.; Ramirez, J.M.; Correa, R.E.; Seminario Anual de Automática, Electrónica Industrial e Instrumentación (SAAEI 2010)

A.4. **A New 84-pulse VSC Configuration Using Multi- Level DC Voltage Reinjection for Especial Applications.-** Valderrábano, A.; Ramirez, J.M.; Correa, R.E.; Industrial Technology (ICIT), 2010 IEEE International Conference on Digital Object Identifier 10.1109/ICIT.2010.5472454

A.5. **A novel VSC behind the StatCom,** Valderrábano, Antonio, Ramirez, Juan M. Electric Power Components and Systems, 1532-5016, Volume 38, Issue 10, 2010, Pages 1161 – 1174. Digital Object Identifier http://dx.doi.org/10.1080/15325001003652918

A.6. **DStatCom regulation by a Fuzzy Segmented PI controller,** Valderrábano, Antonio, Ramirez, Juan M.; Elsevier: Electric Power Systems Research (2009). Digital Object Identifier 10.1016/j.epsr.2009.11.003

A.7. **A DC-DC Multilevel Boost Converter,** Rosas-Caro, J.C.; Ramirez, J.M.; Peng, F.Z.; Valderrabano,A.; Power Electronics, IET Volume 3, Issue 1, January 2010 Page(s):129 – 137. Digital Object Identifier 10.1049/iet-pel.2008.0253

A.8. **An 84-pulse VSC configuration for FACTS devices,** Valderrábano, Antonio, Ramirez, Juan M.; Presented on the International Conference on Industrial Technology (ICIT10), 14-17 March 2010

A.9. **Fixed point DSP-based multi-pulse StatCom voltage control,** Gonzalez, Antonio Valderrabano; Ramirez, Juan M.; Power Symposium, 2008. NAPS '08. 40th North American 28-30 Sept. 2008. Digital Object Identifier 10.1109/NAPS.2008.5307357

A.10. **Voltage balancing in DC/DC multilevel boost converters,** Rosas-Caro, Julio C.; Ramirez, Juan M.; Valderrabano, Antonio; Power Symposium, 2008. NAPS '08. 40th North American 28-30 Sept. 2008 28-30 Sept. 2008 Page(s):1 – 7. Digital Object Identifier 10.1109/NAPS.2008.5307298

A.11. **Details on the implementation of a conventional StatCom's control,** Valderrabano, A.; Ramirez, J.M.;Transmission and Distribution Conference and Exposition: Latin America, 2008 IEEE/PES 13-15 Aug. 2008 Page(s):1 – 7. Digital Object Identifier 10.1109/TDC-LA.2008.4641801

A.12. **Control de Voltaje con un StatCom Multipulso basado en un DSP de punto fijo,** Antonio Valderrábano González, Juan M. Ramírez, Congreso Internacional de Ingeniería Electrónica (CIIE2008), 11-15 Marzo 2008

A.13. **Control de Acondicionadores de Potencia y Dispositivos FACTS,** Julio C. Rosas-Caro, Juan M. Ramírez, Pedro M. García, Antonio Valderrábano, Nojja V. Vanegas Méndez; Congreso Internacional de Ingeniería Electrónica (CIIE2008), 11-15 Marzo 2008

Appendix B

VSC Assembling

On this section a brief explanation of the VSC's development is given along with the bill of materials needed on each board. These boards were designed on Altium Designer 6 (Protel), and the complete set of gerber files verified with CAM350, in order to have a good design for manufacturability. Boards have been hand made on the prototype stage, but the information is complete to build the assemblies in mass production. All these boards are connected together using TMS320F2812 eZdsp DSP Starter Kit (DSK) as the controller board.

B.1. Twelve pulses printed circuit board

The twelve-pulses board has been developed using the intelligent power module (IPM) PM50RLA060 of Powerex as the main device. This device is an isolated base module designed for power switching applications operating at frequencies to 20kHz. Built-in control circuits provide optimum gate drive and protection for the IGBT and free-wheel diode power devices. Table B-1 provides a general Bill of Materials (BOM) for this board. Fig. B.1 12 pulses schematic diagram. illustrates the Schematic electrical diagram for the twelve pulses circuit. It provides opto-coupled isolation for control signals and isolated power supplies for the IPM's built-in gate drive and protection circuits. The interface circuit consists of opto-couplers to transfer control signals and isolated power supplies to power the IPM's internal circuits. The IPM has a common control ground for all three low side IGBTs, which permits the use of a single low side supply so that only four isolated supplies are required. To simplify the design and layout of the required control power supplies we have used Powerex VLA106-24151 isolated DC to DC converter. These DC to DC converters operate from a 24V DC supply and produce an isolated 15V DC output. We used three VLA106-24151 DC to DC converters to provide high side control, and a single VLA106-24151 for the low side control power. The six main IGBT on/off control signals

(UP,VP,WP,UN,VN,WN) are transferred from the system controller to the IPM using high speed optocoupled transistors HCPL-4503.

Fig. B.2, and Fig. B.3, show that the whole circuit can be accomodated in a two layer board, eventhough power planes can be added to preserve signal integrity and reduce unwanted noises.

Table B-1 Bill of Materials for the 12 pulses board.

Bill of Material for 12 PULSOS PM50RLA060_REV3.PRJPCB

On 12/04/2010 at 06:08:08 PM

Comment	Pattern	Quantity	Components	
0.1uF	VP45-3.2	12	C1, C2, C3, C4, C5, C6, C7, C8, C13, C17, C18, C19	Capacitor
1.8K	AXIAL-0.3	2	R17, R25	Resistor
10K	AXIAL-0.3	6	R8, R15, R16, R28, R29, R30	Resistor
150uF	CEL10U	2	C12, C20	Capacitor
15K	AXIAL-0.3	12	R9, R10, R11, R12, R13, R14, R22, R23, R24, R33, R35, R36	Resistor
220	AXIAL-0.3	12	R1, R2, R3, R4, R5, R6, R19, R20, R21, R27, R31, R32	Resistor
39uF	CEL10U	6	C9, C10, C11, C14, C15, C16	Capacitor
4.7K	AXIAL-0.3	4	R7, R18, R26, R34	Resistor
CONN_8	POWER-8	1	J6	POWER CONNECTOR
DC_JACK	DC_JACK - PJ038A	1	JP2	Header, 3-Pin
HCPL-4503	DIP-8	12	U1, U2, U3, U4, U5, U6, U8, U13, U14, U18, U19, U20	HCPL-4503
HDR2X20	HDR2X20	1	JP1	Header, 20-Pin, Dual row
LED1	LED-1	2	D1, D2	Typical RED GaAs LED
MC74HCT573AN	738-03	2	U23, U24	Octal 3-State Non-Inverting Transparent Latch with LSTTL-Compatible Inputs
PM50RLA060	PM50RLA060	2	U7, U22	PM50RLA060
VLA106-24151	VLA106-24151	8	U9, U10, U11, U12, U15, U16, U17, U21	VLA106-24151
PCB	PCB	1	PCB	Printed Circuit Board

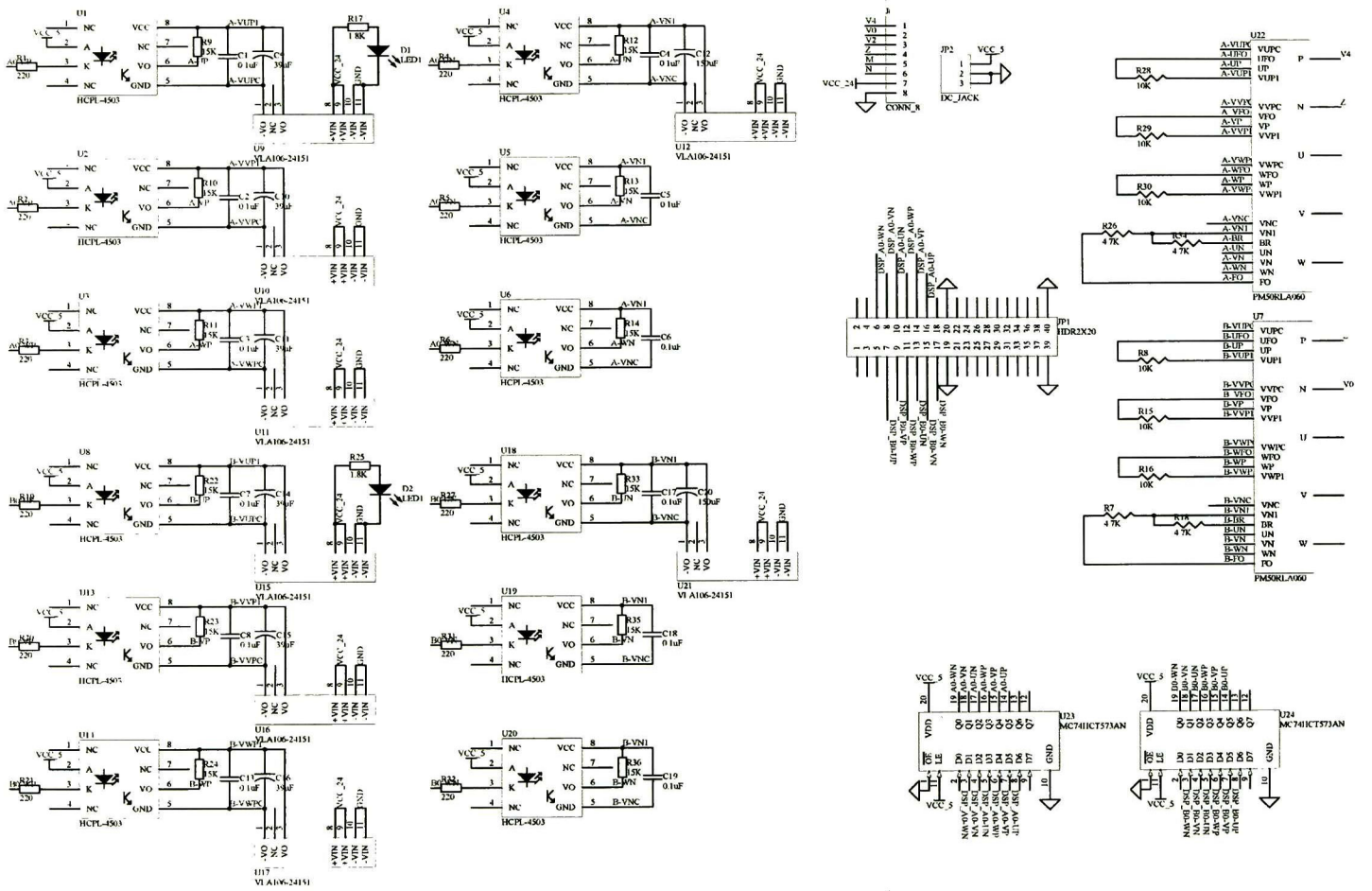

Fig. B.1 12 pulses schematic diagram.

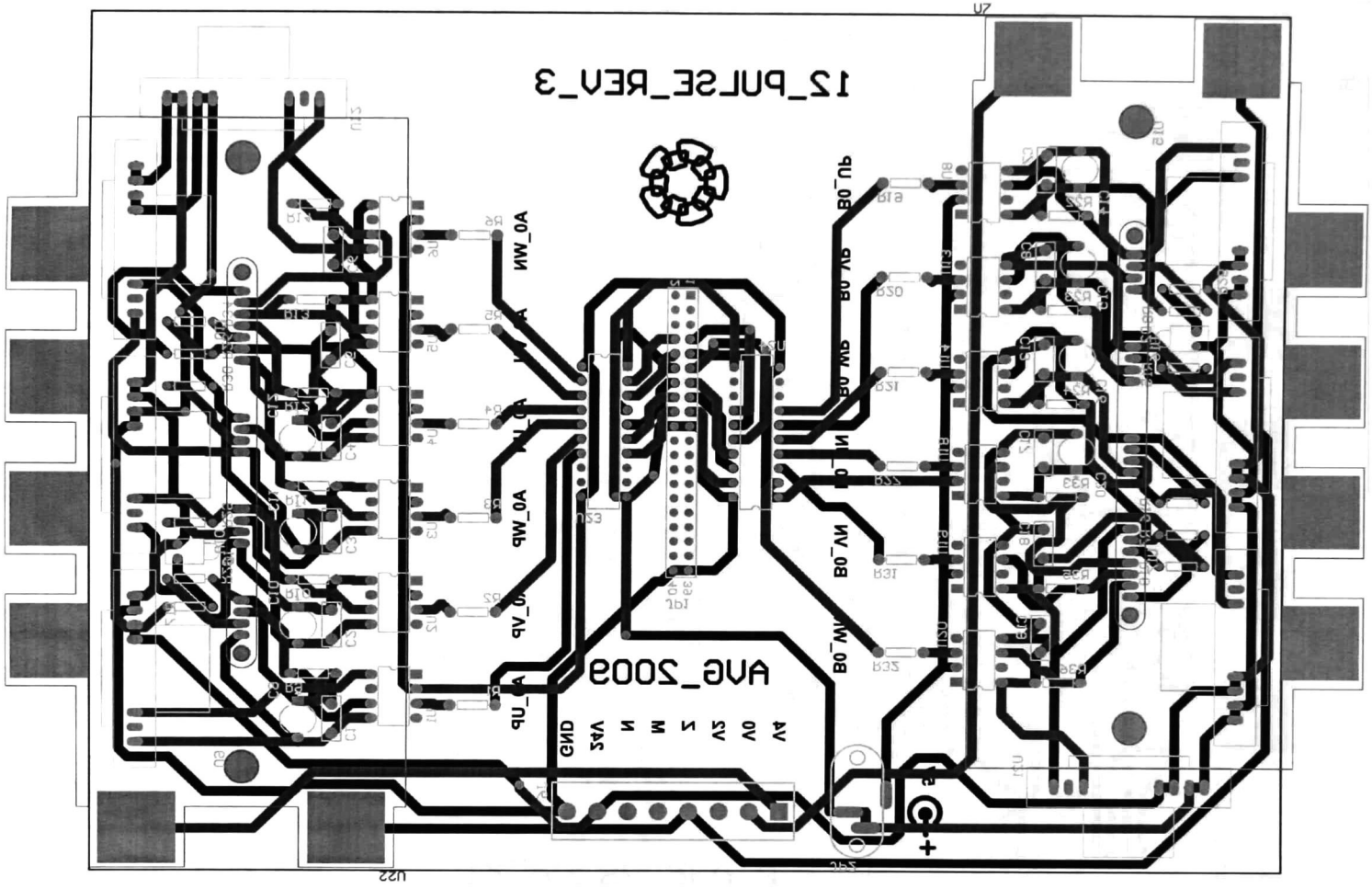

Fig. B.2 12 pulses Printed Circuit Board view from Bottom Side.

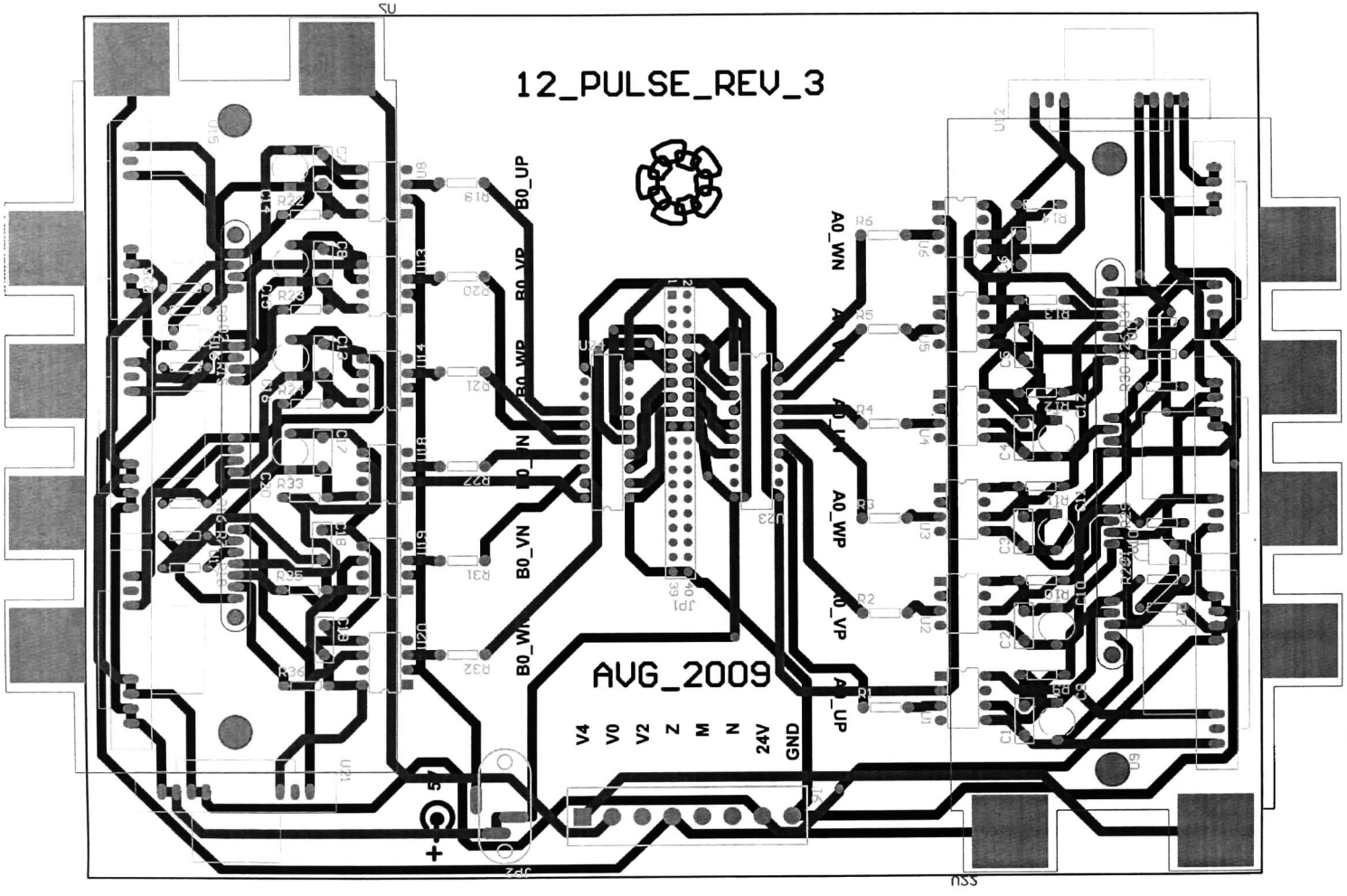

Fig. B.3

12 pulses Printed Circuit Board view from Top Side.

B.2. Seven-level printed circuit board

The seven level uses single IGBT chips IRG4RC10SD with ultrafast diode. Table B-2 provides a general Bill of Materials (BOM) for this board. We have used the same kind of optocouplers and DC to DC converters than used for twelve pulses board for design simplification. Fig. B.4 7 level Schematic diagram. depicts the Schematic electrical diagram for seven level circuit.

Fig. B.5 7 level Printed Circuit Board view from Bottom Side.and Fig. B.6 are used to demonstrate that the whole circuit can be accomodated also in a two layer board. Power planes can be added to preserve signal integrity and reduce unwanted noise.

Table B-2 Bill of Materials for 7 level board

Bill of Material for 7_LEVEL.PrjPcb				
On 12/04/2010 at 05:51:56 PM				
Comment	**Pattern**	**Quantity**	**Components**	
0.1uF	VP45-3.2	9	C1, C2, C3, C4, C9, C10, C11, C12, C27	Capacitor
0	AXIAL-0.3	1	R18	Resistor jumper
10uF	CEL10U	13	C5, C6, C7, C8, C13, C14, C15, C16, C26, C28, C29, C30, C31	Capacitor
15K	AXIAL-0.3	8	R5, R6, R7, R8, R13, R14, R15, R16	Resistor
220	AXIAL-0.3	8	R1, R2, R3, R4, R9, R10, R11, R12	Resistor
2200uF	CEL10U	1	C25	Capacitor
3.3	AXIAL-0.5	1	R17	Resistor
CON2	POWER-2	5	J1, J2, J3, J4, J5	Connector
CONN_8	POWER-8	1	J6	POWER CONNECTOR
DC_JACK	DC_JACK	1	JP2	DC power jack
HCPL-4503	DIP-8	8	U1, U2, U3, U4, U9, U10, U11, U12	HCPL-4503
HDR2X20	HDR2X20	1	JP1	Header, 20-Pin, Dual row
IRG4RC10SD	TO-252AA	8	Q1, Q2, Q3, Q4, Q6, Q7, Q8, Q9	Insulated Gate Bipolar Transistor with Ultrafast Soft

				Recovery Diode
M57140-01	M57140-01	1	U22	M57140-01
MC74HCT573AN	738-03	1	U23	Octal 3-State Non-Inverting Transparent Latch with LSTTL-Compatible Inputs
MURS320T3	SMC	4	D1, D2, D3, D4	Default Diode
TIP2955	TIP2955	1	Q5	PNP Bipolar Transistor
VLA106-24151	VLA106-24151	8	U5, U6, U7, U8, U13, U14, U15, U16	VLA106-24151
VOLTREG	TO-220	1	U21	Voltage Regulator
PCB	PCB	1	PCB	Printed Circuit Board

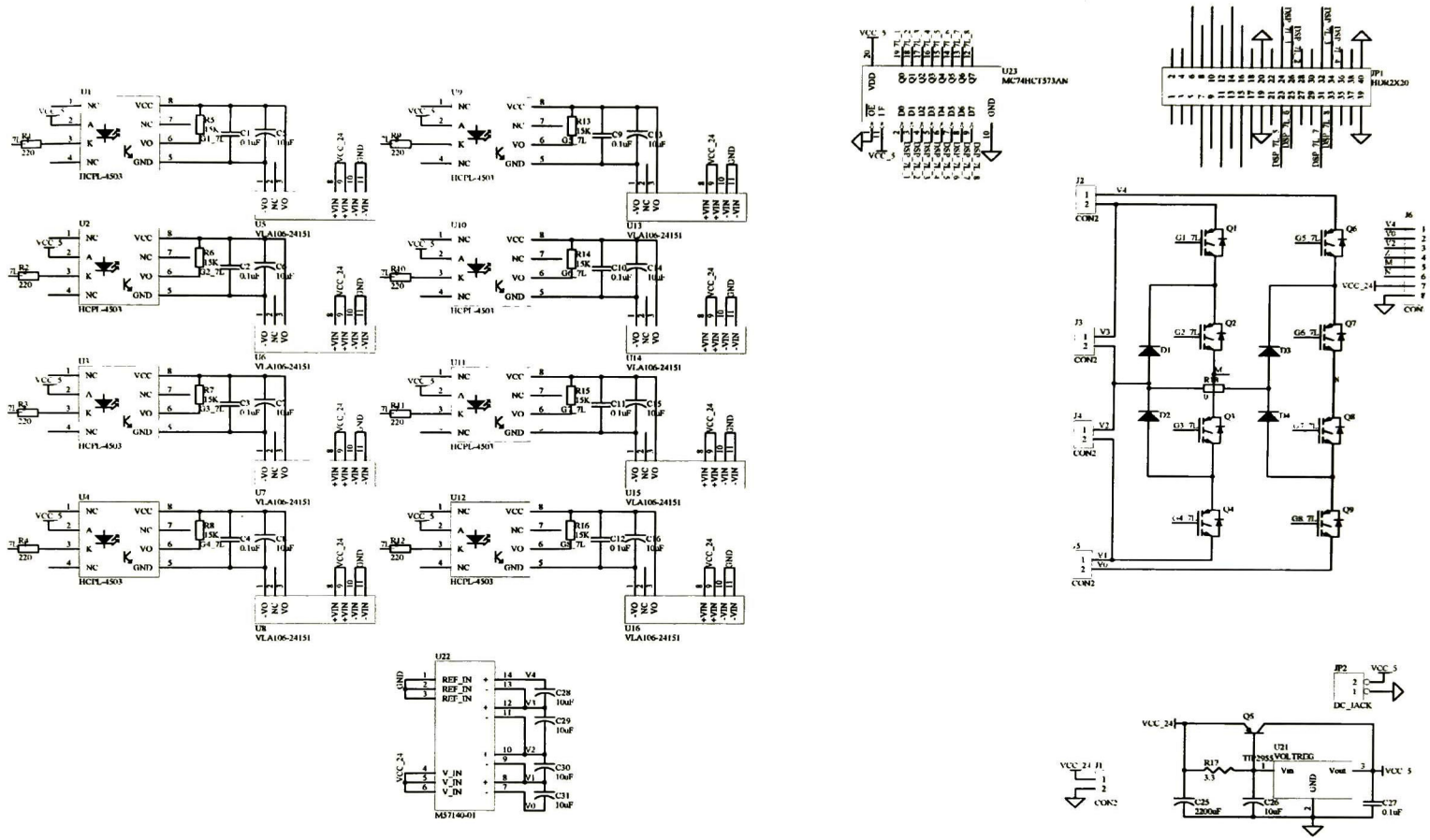

Fig. B.4 7 level Schematic diagram.

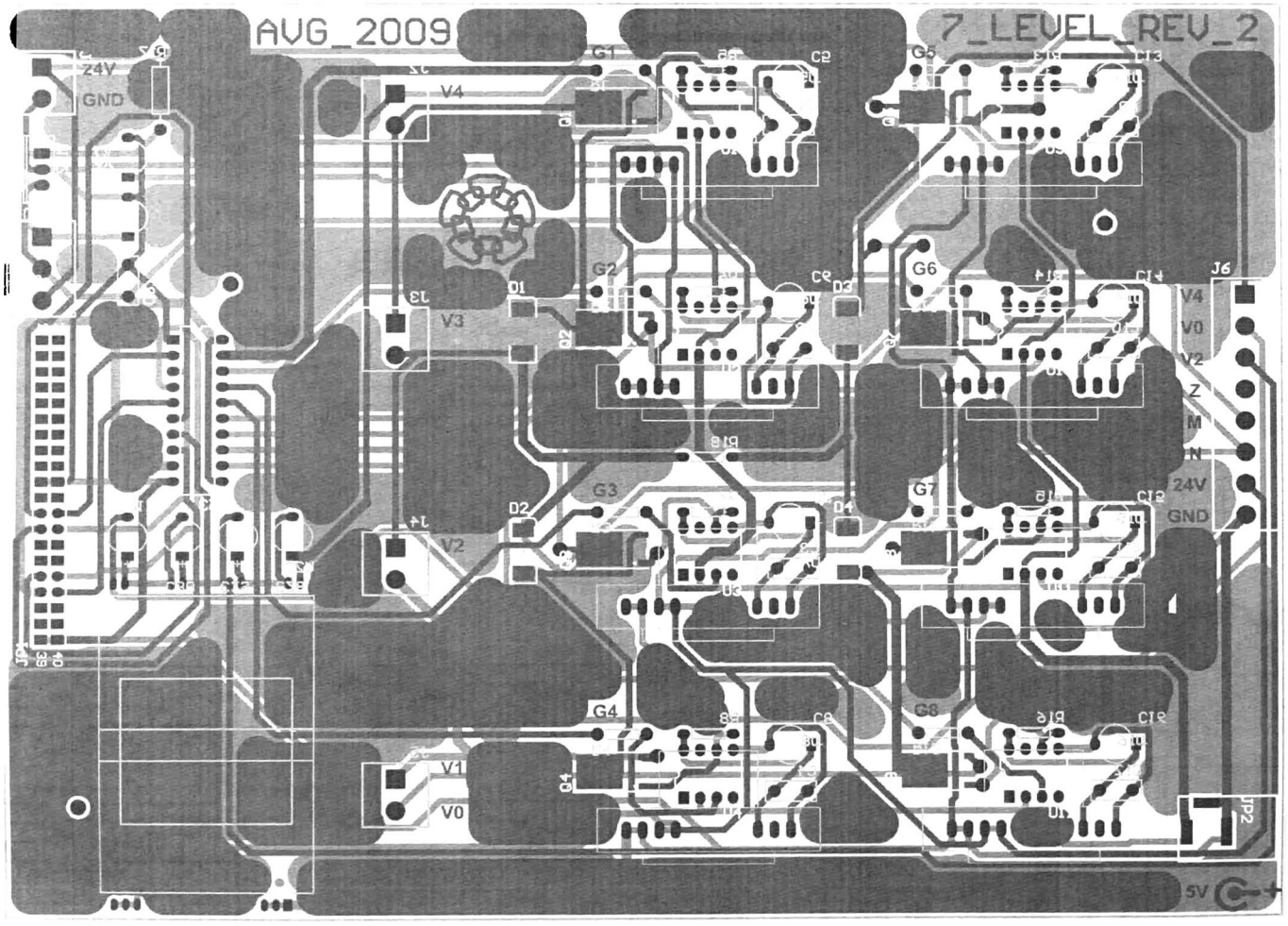

Fig. B.5 7 level Printed Circuit Board view from Bottom Side.

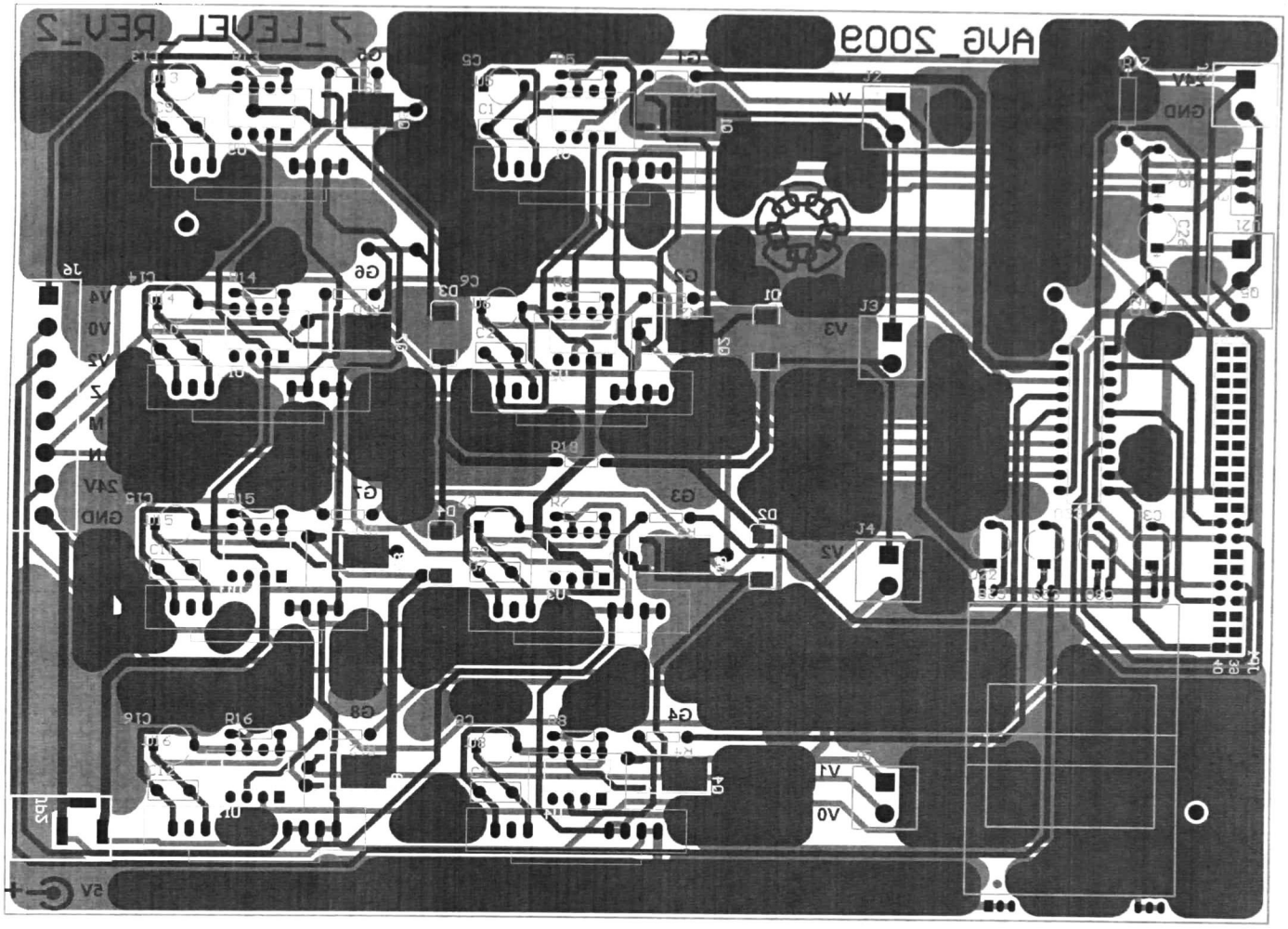

Fig. B.6 7 level Printed Circuit Board view from Top Side

B.3. Signal conditioning printed circuit board

Very important is to take into account the voltage levels of the transmission line. On the built prototype, the maximum voltage to be read is 268 VRMS line. Since we are using TMS320F2812 Digital Signal Processor (DSP) as the core for the control stage, we have to this RMS voltage corresponds to 0-3V for the input of the ADC of the TMS320F2812 DSP. That is why the array presented on Fig. B.7 is used. We are using a ΔY array on the signal transformators VPP10-250 to have a major reduction on the secondary side. Each phase on the secondary side is passed through a INA159, which has gain of 0.2 in order still have a lower voltage at the output and uses a REF2930 chip to have the 3V needed at the input of the ADC at full scale, having zero volts of the AC line mounted on 1.5 volts at the input of the ADC. This board includes also a signal conditioner circuit for current based on ACS712 Hall Effect-Based Linear Current Sensor IC. The general Bill of materials is included on, and the single layer printed circuit board on Fig. B.8 Signal Conditioner Printed Circuit Board view from Bottom Side.

Table B-3 Bill of Materials for Signal Conditioning board

Bill of Material for SIGNAL CONDITIONER_line.PrjPcb				
On 12/04/2010 at 05:36:52 PM				
Comment	**Pattern**	**Quantity**	**Components**	**Description**
0.1uF	RAD-0.2	6	C1, C2, C3, C4, C5, C6	Capacitor
1k	AXIAL-0.4	3	R1, R2, R3	Resistor
10k	AXIAL-0.4	3	R16, R17, R18	Resistor
12k	AXIAL-0.4	6	R7, R8, R9, R10, R11, R12	Resistor
15k	AXIAL-0.4	3	R13, R14, R15	Resistor
180	AXIAL-0.4	3	R4, R5, R6	Resistor
ACS712	751-05_L	3	U13, U14, U15	Current Sensor
DC_JACK	POWER_JACK	2	JP2, JP5	DC power jack
Header 3	HDR1X3	2	JP3, JP4	Header, 3-Pin
Header 3	POWER-3	3	P1, P2, P3	Header, 3-Pin
HEADER 4	HDR1X4	1	JP1	4 Pin Header
INA159	MSOP8	6	U1, U2, U3, U7, U8, U9	Opamp Divider
LM324AD	751A-03_L	1	U16	Quad Differential Input, Low-Power Operational

				Amplifier
REF2930	SOT-23	6	U4, U5, U6, U10, U11, U12	Voltage Reference
Transformer	VPP10-250	6	T1, T2, T3, T4, T5, T6	Signal Transformer
PCB	PCB	1	PCB	Printed Circuit Board Signal Conditioner

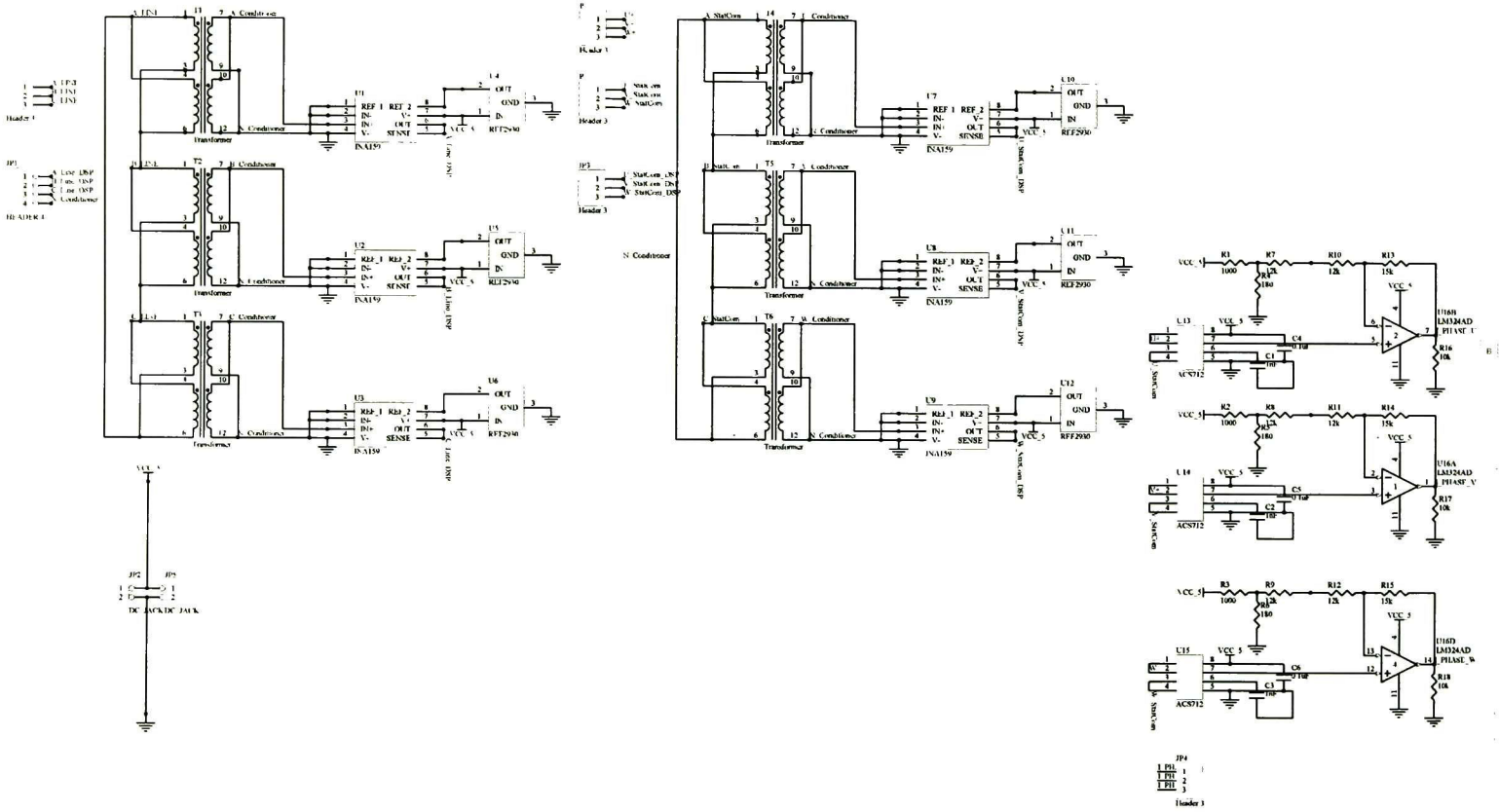

Fig. B.7 Signal Conditioner Schematic diagram.

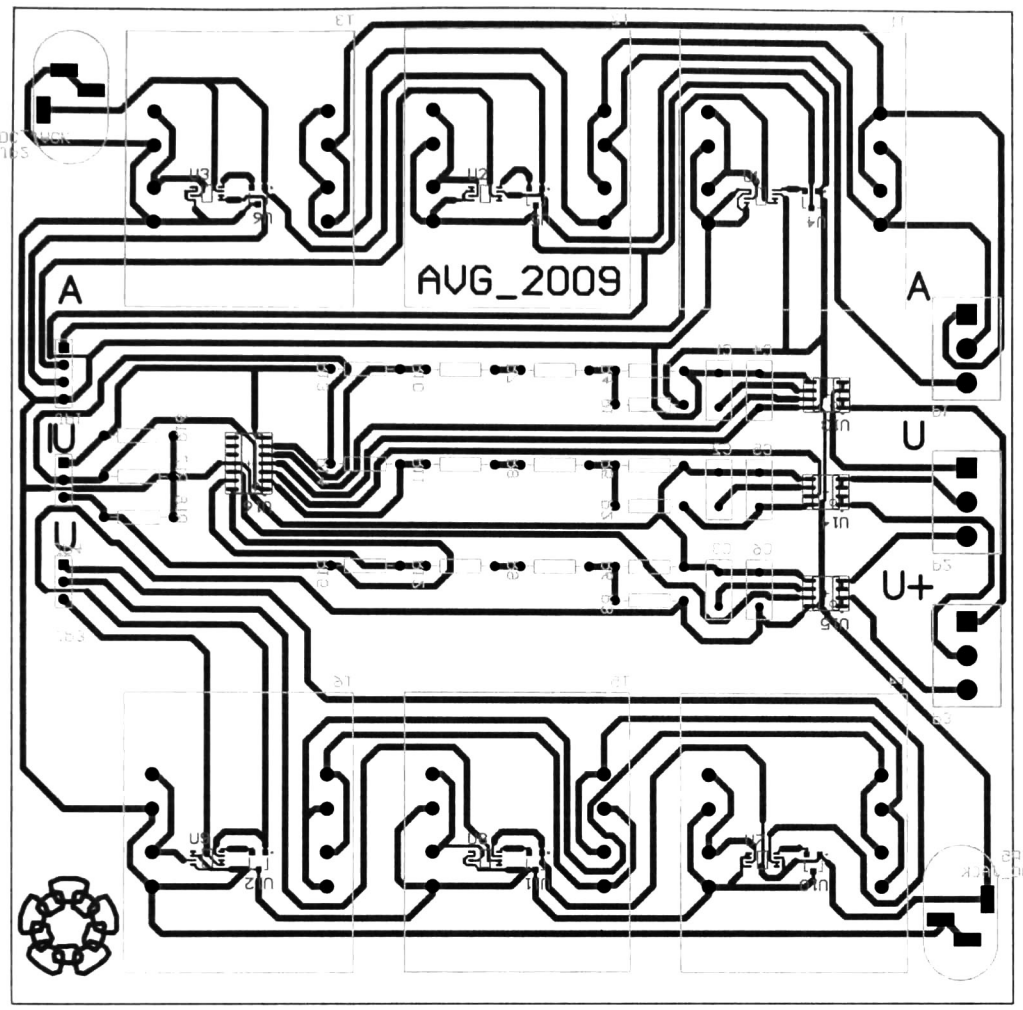

Fig. B.8 Signal Conditioner Printed Circuit Board view from Bottom Side

B.4. VSC connected as StatCom with energy source

The diagram of the Fig. 2.3 has been built as a prototype. Fig. B.9 **VSC assembly**depicts the main components of the VSC. The eZdsp TMS320F2812 receives the voltage and current signals from the signal conditioner printed circuit board, processes them, and proportionates the appropriate gate signals to the seven level board and to the twelve pulses board, through the 40 line IDE cable. 20 to 24 Volts are provided to each of the DC to DC converters to provide isolated voltage to the IGBTs gate. Seven level signals are rised through 4 different DC sources, which would be replaced by capacitors. They are direct connected to the seven level's board; the

output is sent to reinjection transformer. The output of the reinjection transformer is fed to the seven level board to complete the process, and the output is fed to twelve pulses board. The two IPM blocks are responsible to modify the signal according to Fig. 2.4, having the output presented on Fig. 4.4 and Fig. 4.3. These outputs are added on the three phase transformers of Fig. B.10, obtaining the VSC outputs in Fig. 4.8.

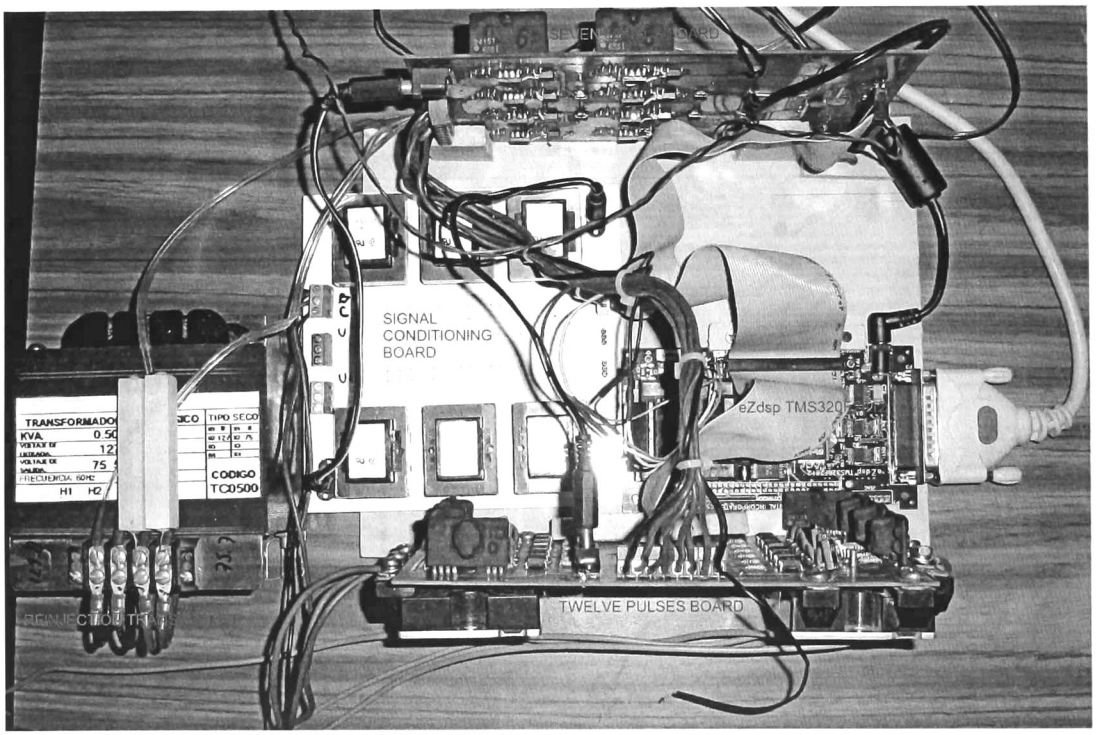

Fig. B.9 VSC assembly

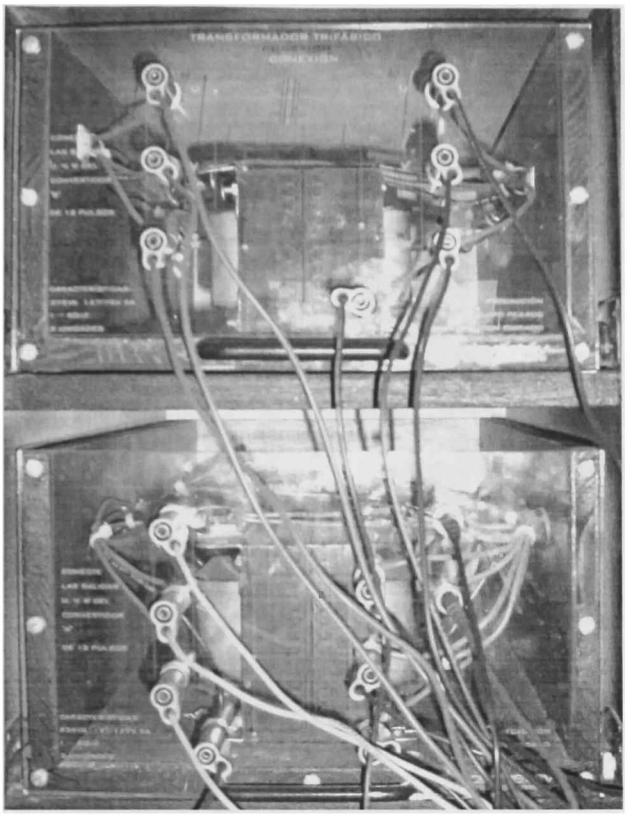

Fig. B.10 Three phase transformer array

The whole StatCom array is presented on Fig. B.11.

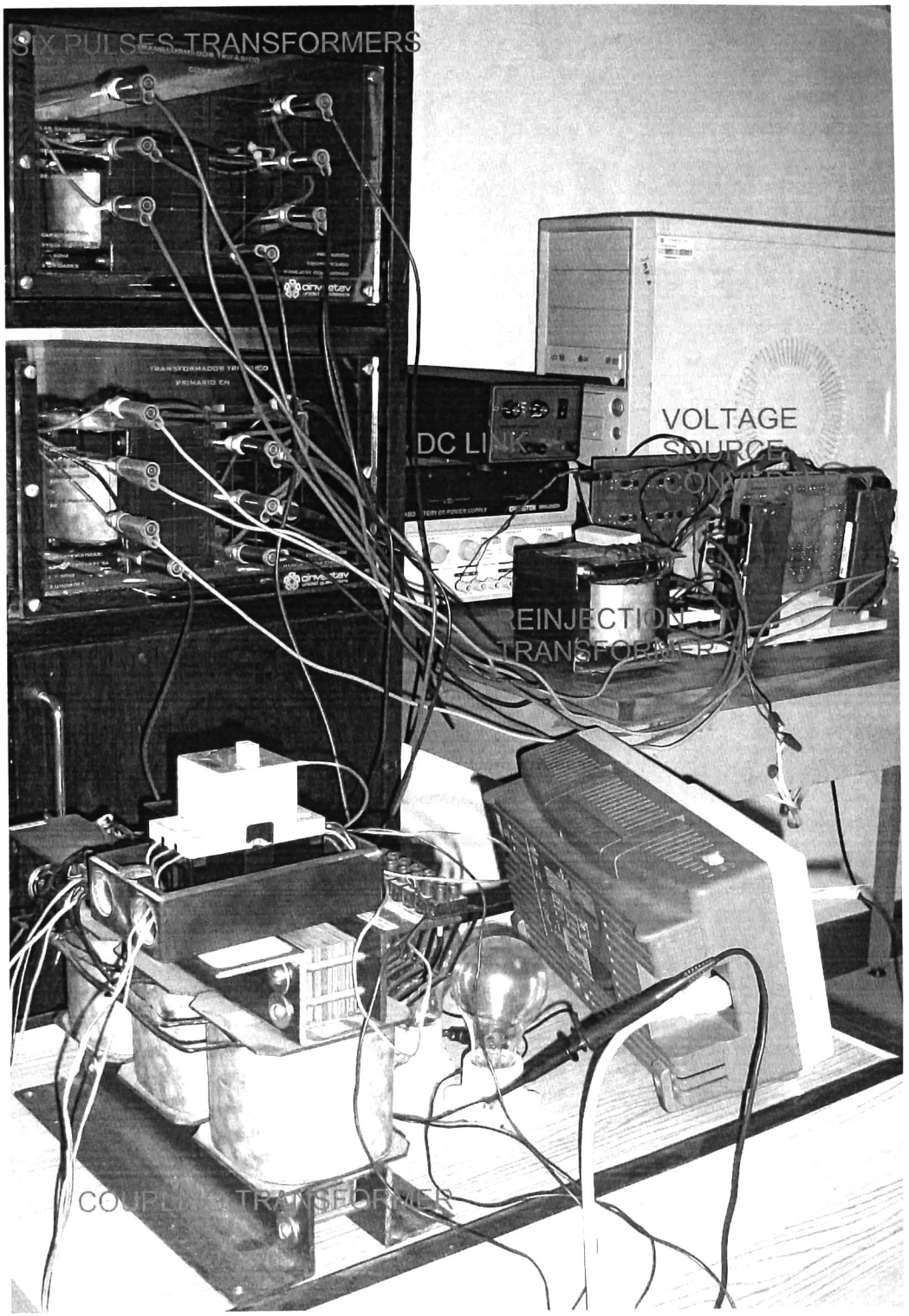

Fig. B.11 StatCom Prototype

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El Jurado designado por la Unidad Guadalajara del Centro de Investigación y de Estudios Avanzados del Instituto Politécnico Nacional aprobó la tesis

Diseño e Implementación de un Convertidor de 84 Pulsos
84-Pulses Converter: Design and Assembling

del (la) C.

Antonio VALDERRÁBANO GONZÁLEZ

el día 16 de Diciembre de 2010.

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